KEYSIGHT

High-Speed Digital TX & RX Fundamentals and Debug Techniques

Thomas Giehm
High-Speed Digital Solutions

High-Speed digital systems overview

What are they and when do we use them?

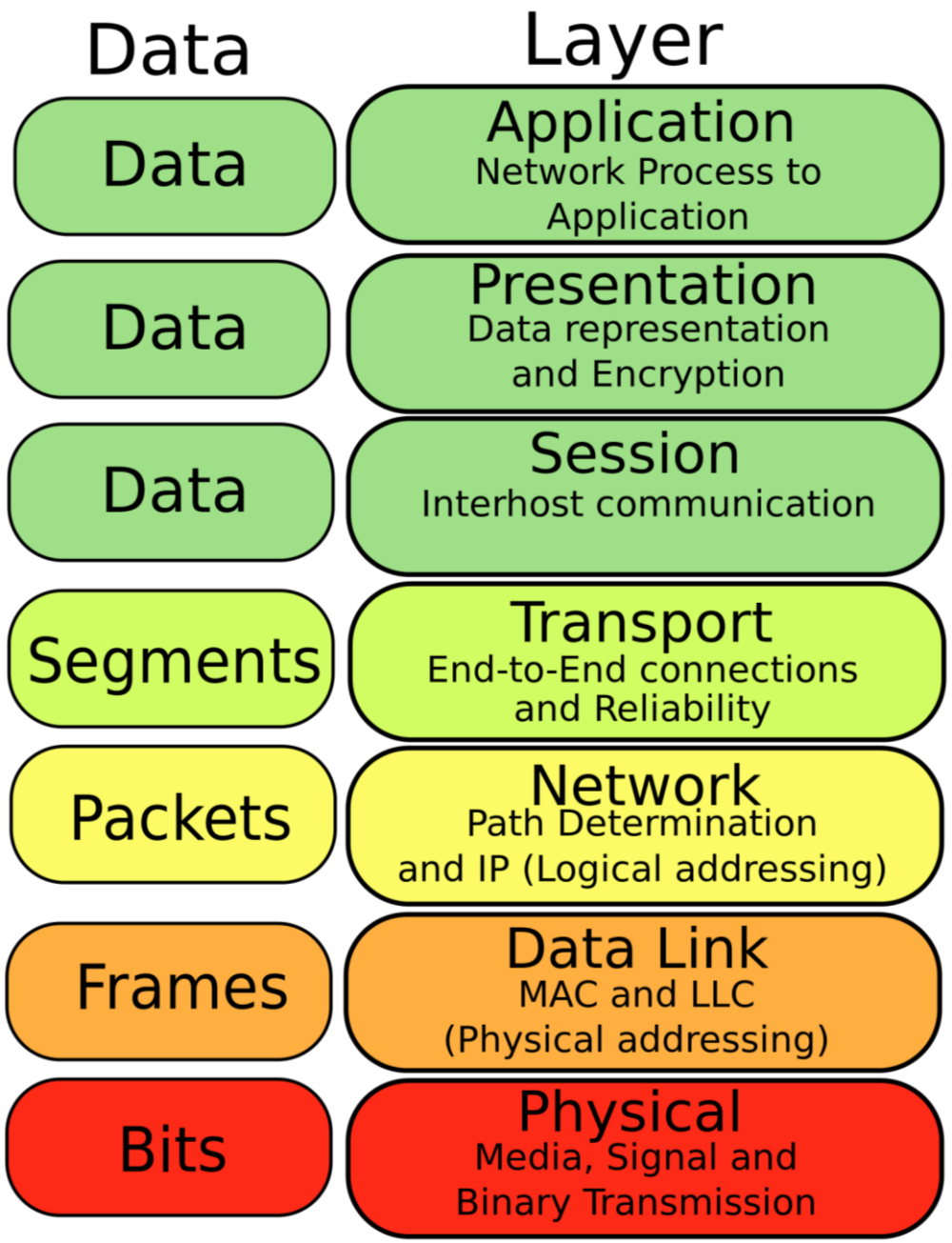
- Systems that process and transmit digital signals at high frequencies
- Involve precise timing, signal integrity, and high-bandwidth communication
- Increased Data Demand, Compact and Efficient Designs, Reliability in Critical Applications
- Examples: PCIe, USB, Ethernet(including Automotive Ethernet), and memory interfaces (DDR)



High-Speed Digital Systems: OSI Model

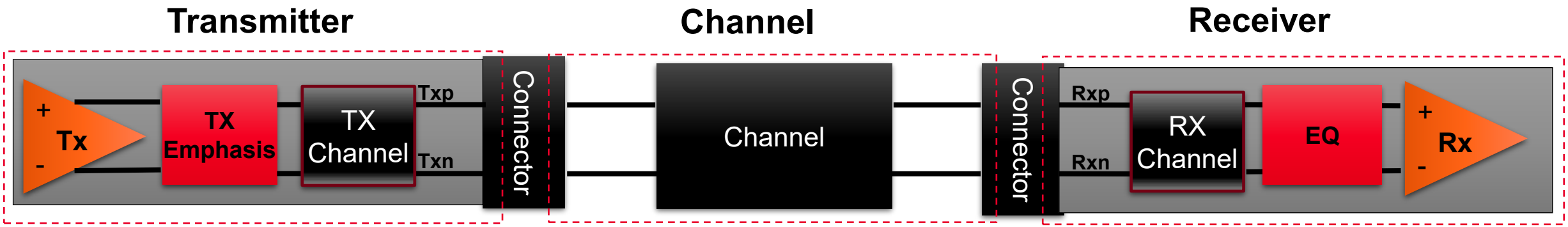
Physical Layer

- The OSI (Open Systems Interconnection) model is a framework for standardizing communication in networks
- **The Physical Layer**, the foundation where electrical, optical, or wireless signals transmit raw data
- Signal encoding and modulation
- Media type and transmission speed definition (e.g., cables, PCBs, optical fibers)
- Synchronization, voltage levels, and data rates



Serial Data Link Overview

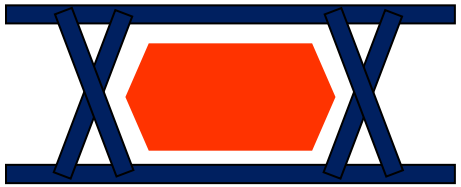
Typical Physical Layer Link



- **Transmitter** - Buffers signal for transmission outside of IC
  - Output tests verify transmitted signal quality
- **Channel** - Passive interconnect between ICs. Circuit board trace, connectors, backplane…
  - Often differential
  - Impedance through, signal reflection, crosstalk coupling
- **Receiver** – Detects, retimes, and “cleans up” signal
  - Input tests determine receiver’s ability to recover impaired signal

Characterizing Transmitters versus Receivers

Transmitters



Usually eye diagram based - Measured with a scope

- Quick
- Intuitive
- Often involves testing against a mask

Receivers

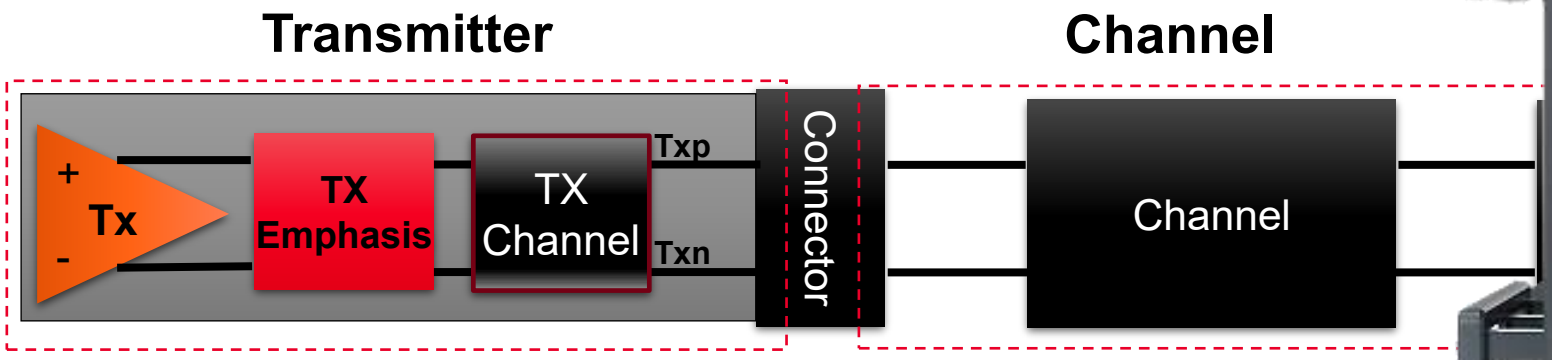
Bit Error Ratio (BER) based:

- Output waveform of receiver gives no clue about whether errors were made
- Measuring that correct decisions were made
- Frequently also how well clock recovery is performing
- Less intuitive

Serial Data Link Overview

Transmitter (TX) Testing

What is the best tool for analyzing the performance of a transmitter?



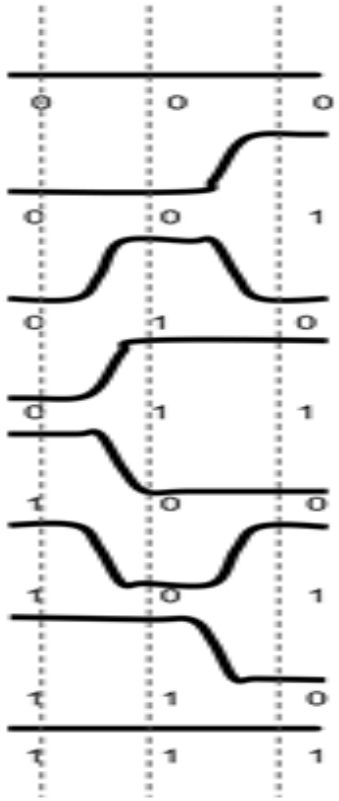


- Low noise to measure TX signal quality without impacting the signal
- Ability to add/remove channel effects
- Can act as an ideal receiver or as real-world receiver

Transmitter Testing

Real Time Eye Diagram

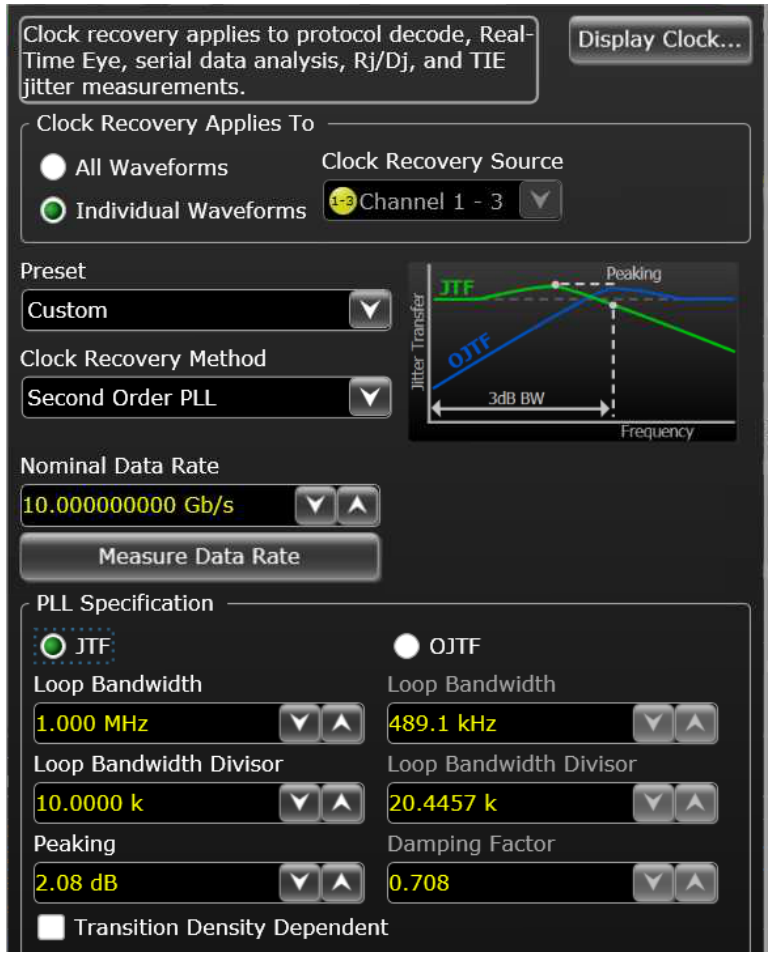
- Eye diagrams are a layered view of every bit transition combination
- There are eight of these in total
- Each of these are layered to make up the eye
- This provides a composite picture of the overall quality of a system's physical layer characteristics like
  - amplitude variation
  - timing uncertainties
  - infrequent glitches
- With more acquisition data, you can get a more complete picture of the jitter, anomalies, or other infrequent events that are present





Transmitter Testing

Real Time Eye and Clock Recovery



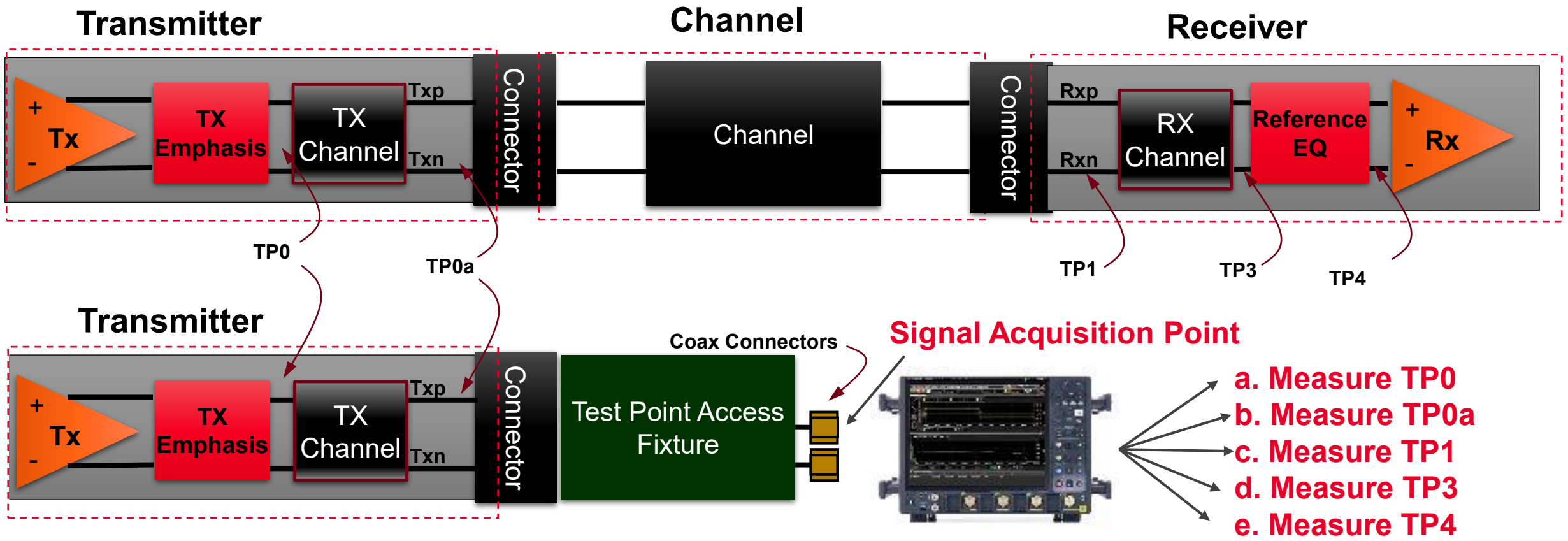
- Clock recovery is the process of extracting a clock from an incoming data signal.
- Most receivers implement some type of clock recovery in order to retime data.
- Clock recovery implementations can be used to reduce or remove timing jitter.
- Loop bandwidth is used to define the jitter transfer function (JTF, sampling scopes) or observed jitter transfer function (OJTF, RT scope).
  - JTF - Jitter Transfer Function
    - How much of the jitter on the input signal is “transferred” to the recovered clock.
    - Low pass filter function
  - OJTF – Observed Jitter Transfer Function
    - How much jitter will be “observed” by the receiver
    - High frequency jitter on data stream is transferred to RX.

Embedding and De-Embedding

Measurement Point Location, Possible Scenarios, Transfer Functions, Channel Element Models

Another Fundamental Challenge

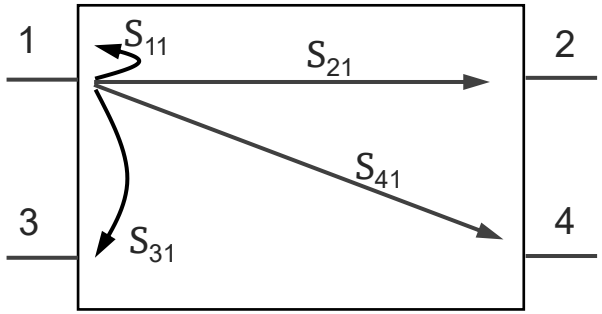
The Test Point For Measurement Is NOT Where The Oscilloscope Is Connected!



Removing the effects of circuit blocks is commonly called De-embedding and Adding effects of circuit blocks is called Embedding.

Measurement with De-embedding & Embedding

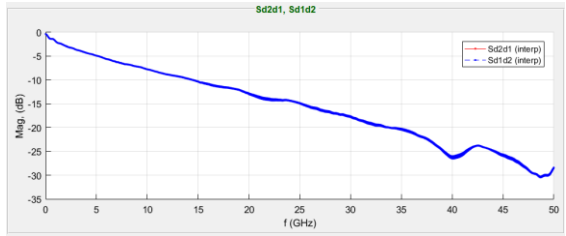
If we have S-parameter models for these circuit blocks we can do signal processing in the oscilloscope to account for these. 4 Port S-parameters to describe differential structures.

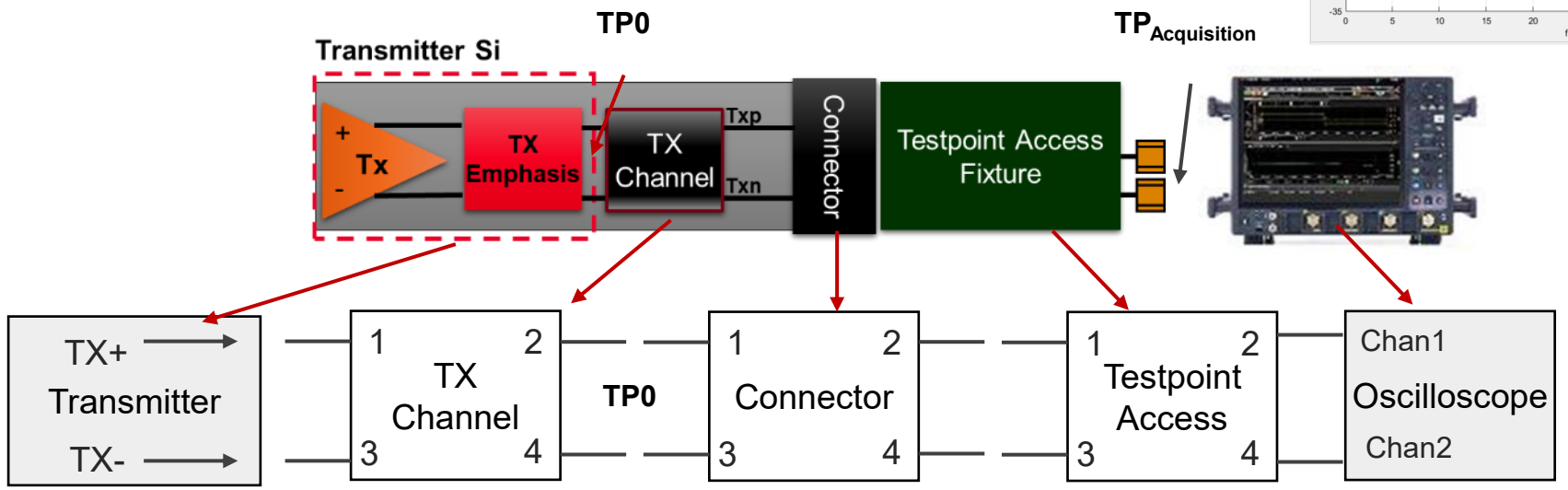


$$\begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{21} & S_{22} & S_{21} & S_{24} \\ S_{31} & S_{32} & S_{33} & S_{24} \\ S_{41} & S_{42} & S_{43} & S_{44} \end{bmatrix}$$

There are 16 complex values at every frequency that define the performance of the network.

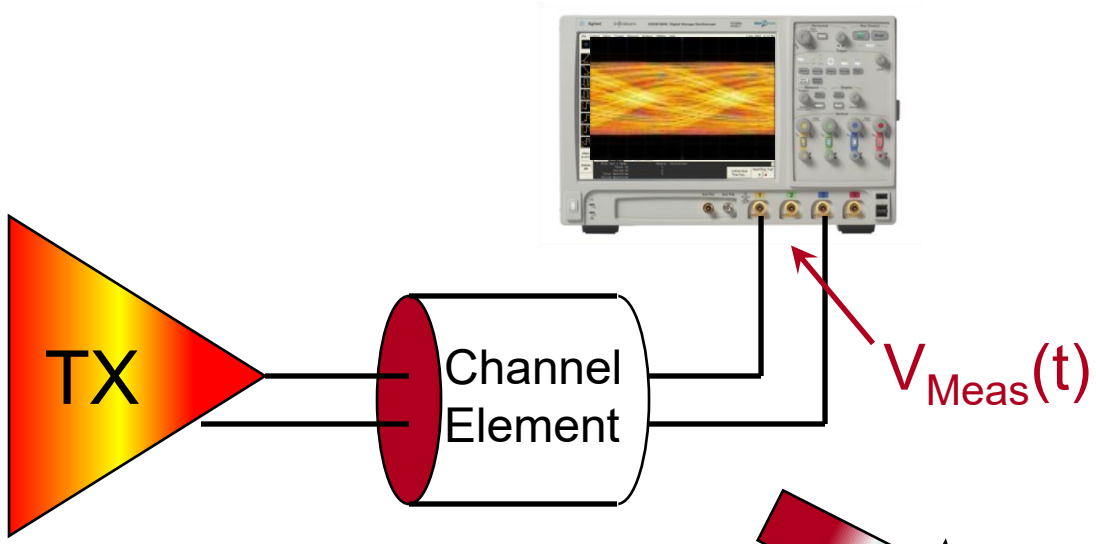
S_{21}



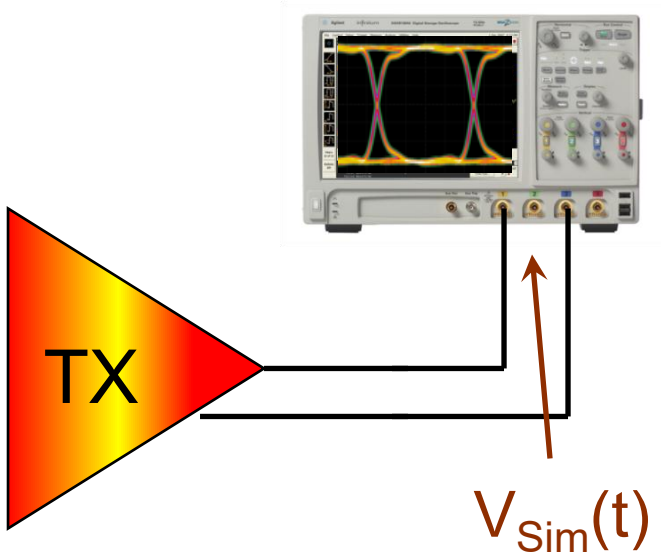


In this example, we can measure the signal at TP0 by creating a transfer function that relates $TP_{Acquisition}$ to TP0.

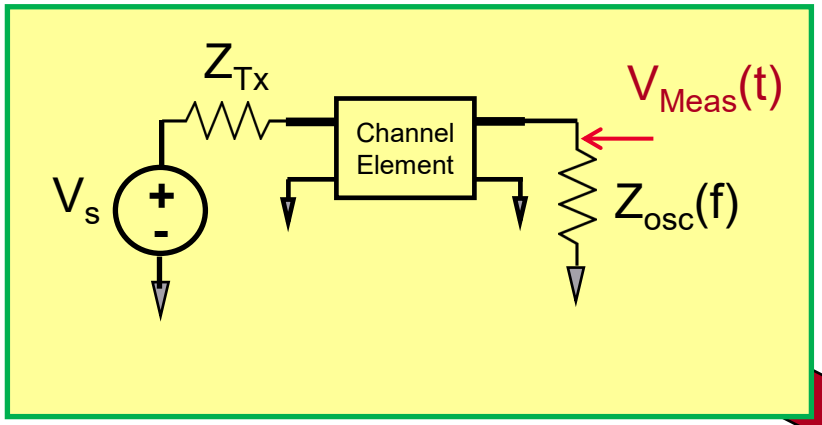
De-embedding → Channel Element Removal



Examples:
- Test Fixtures
- Cables
- Connectors
- Lossy PC boards

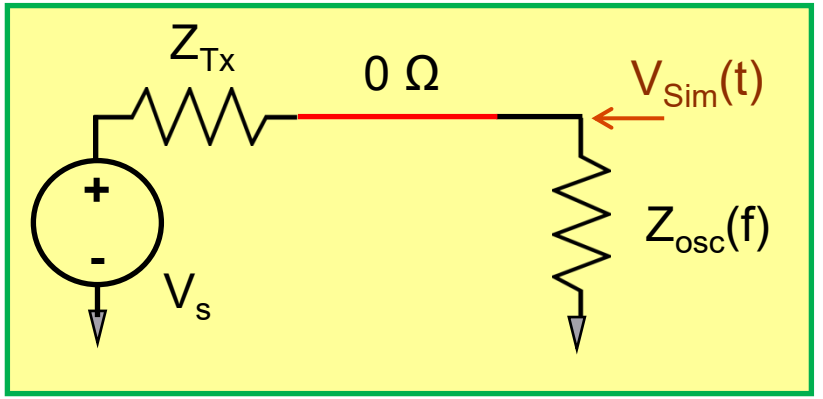


De-embedding → Channel Element Removal

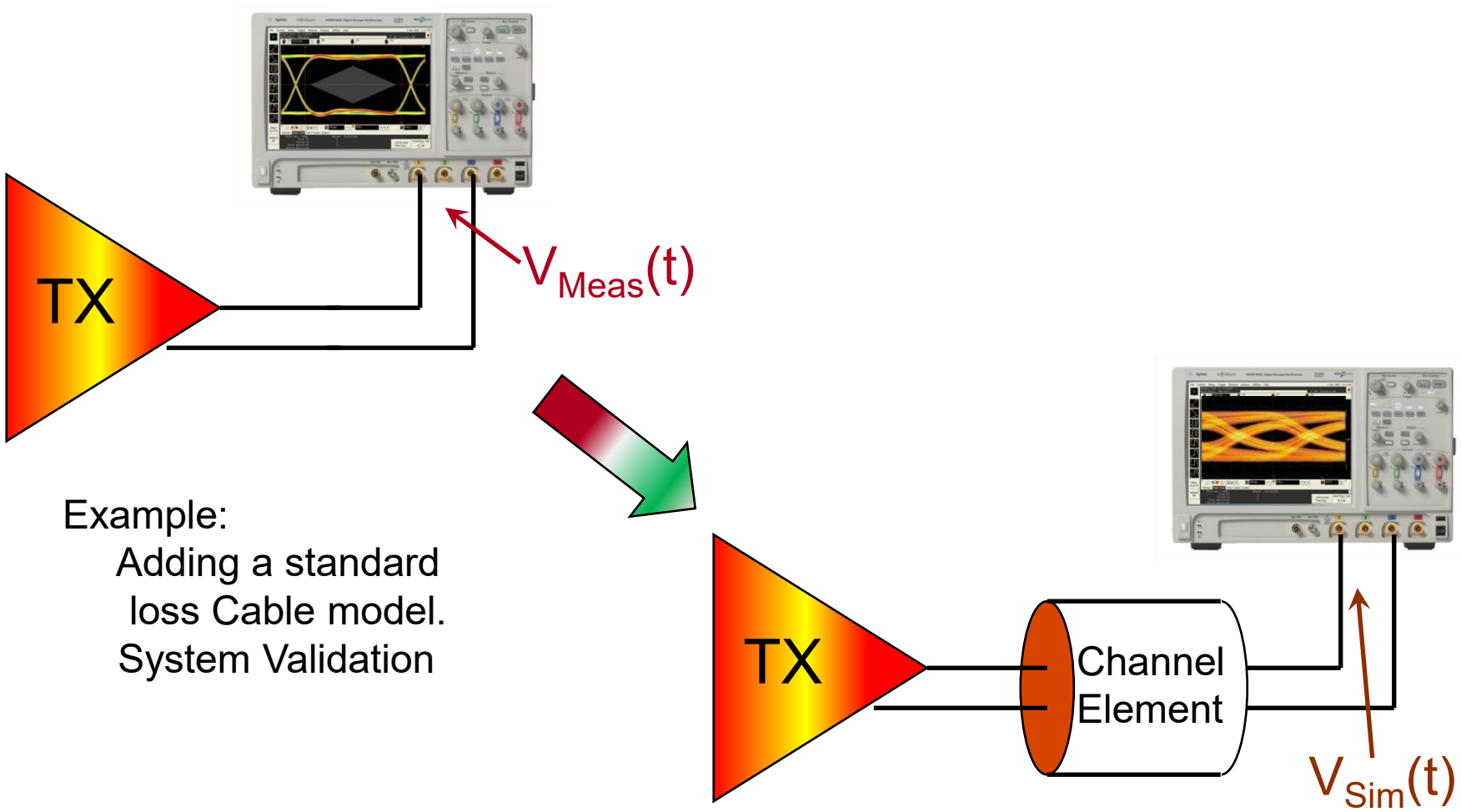


Examples:

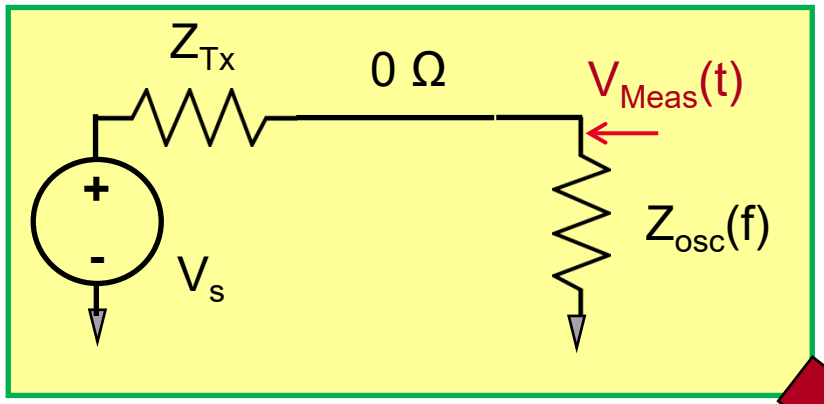
- Test Fixtures
- Cables
- Connectors
- Lossy PC boards



Embedding → Channel Element Insertion



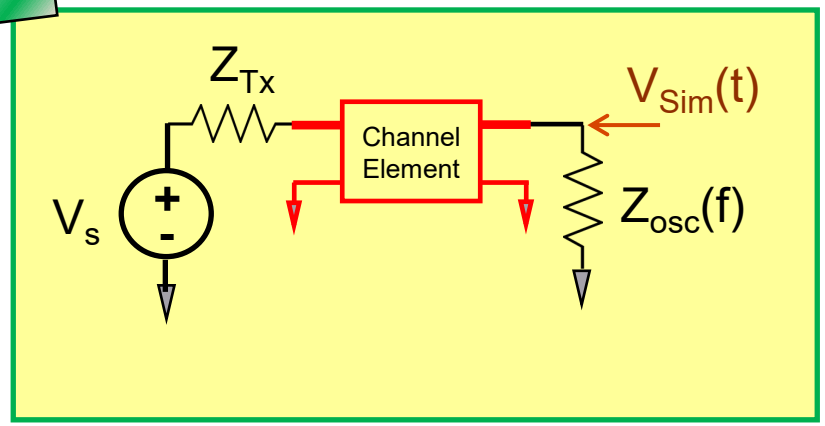
Embedding→ Channel Element Insertion



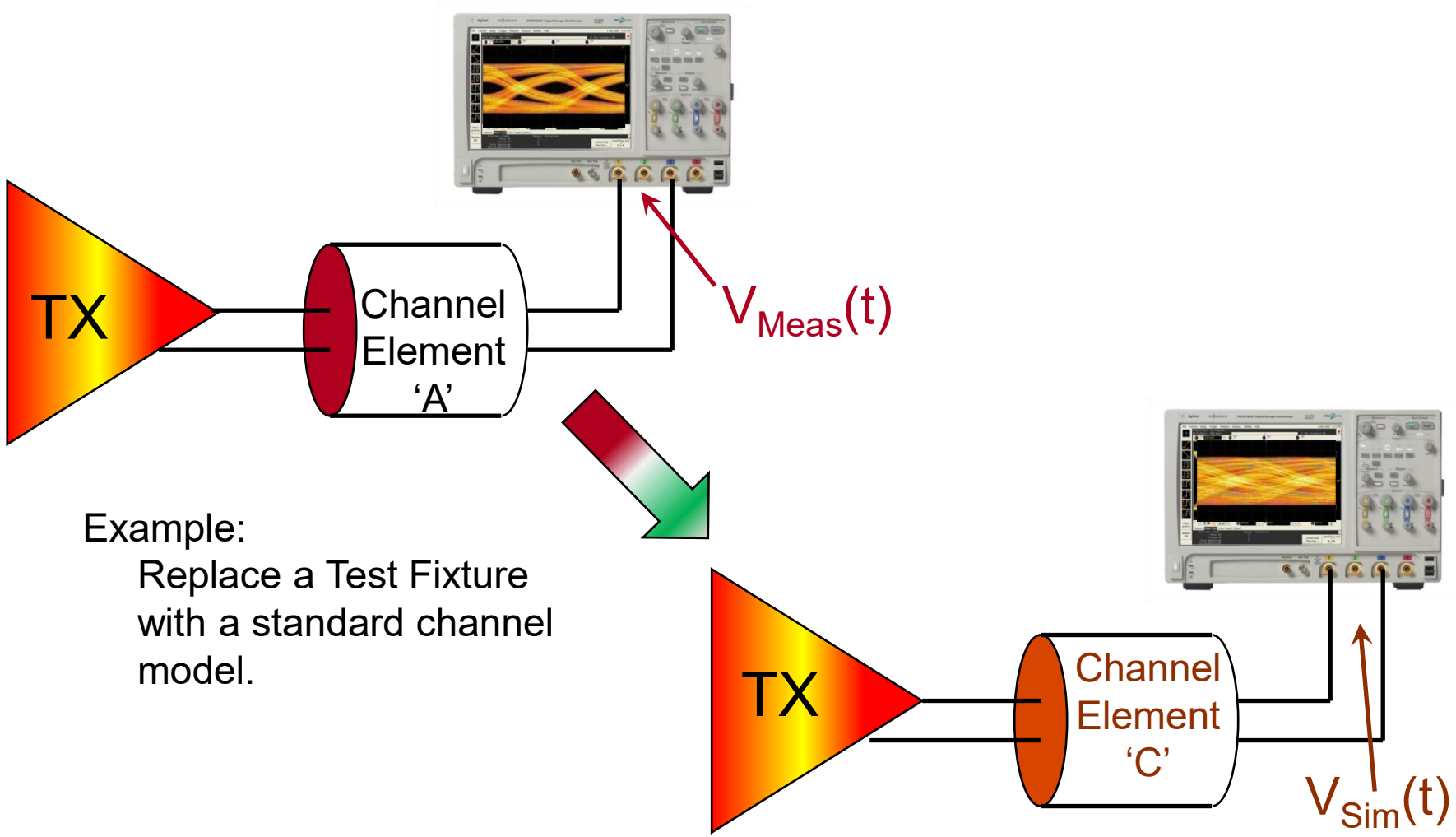
Example:

Adding a standard loss Cable model.

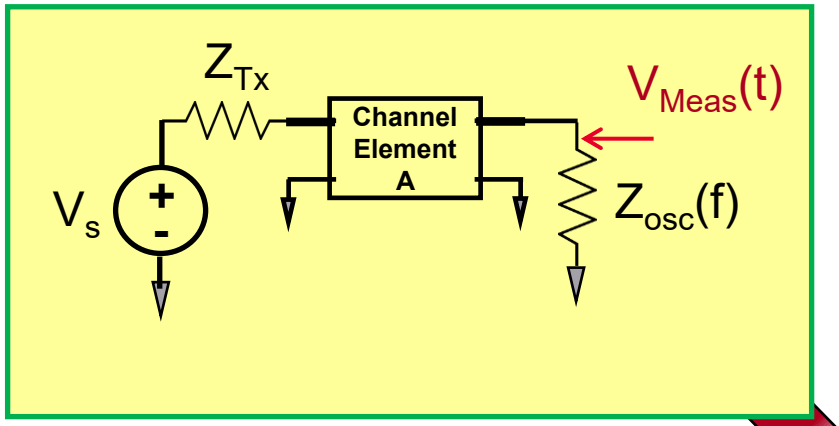
System Validation



Combination of De-embedding & Embedding → Channel Element Replacement

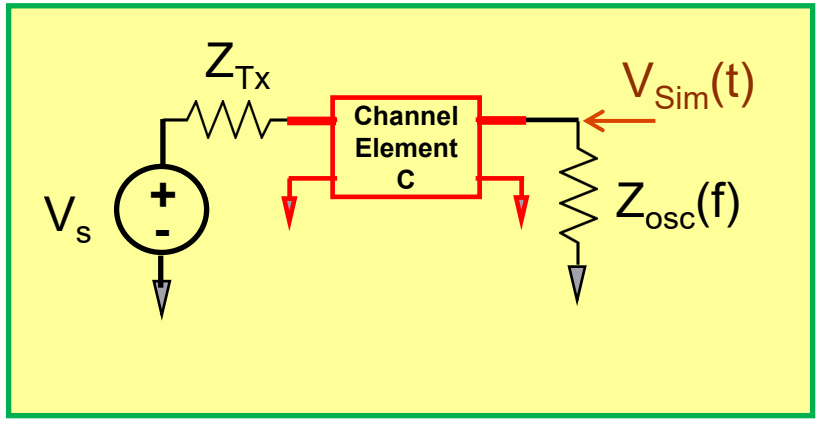


Combination of De-embedding & Embedding → Channel Element Replacement



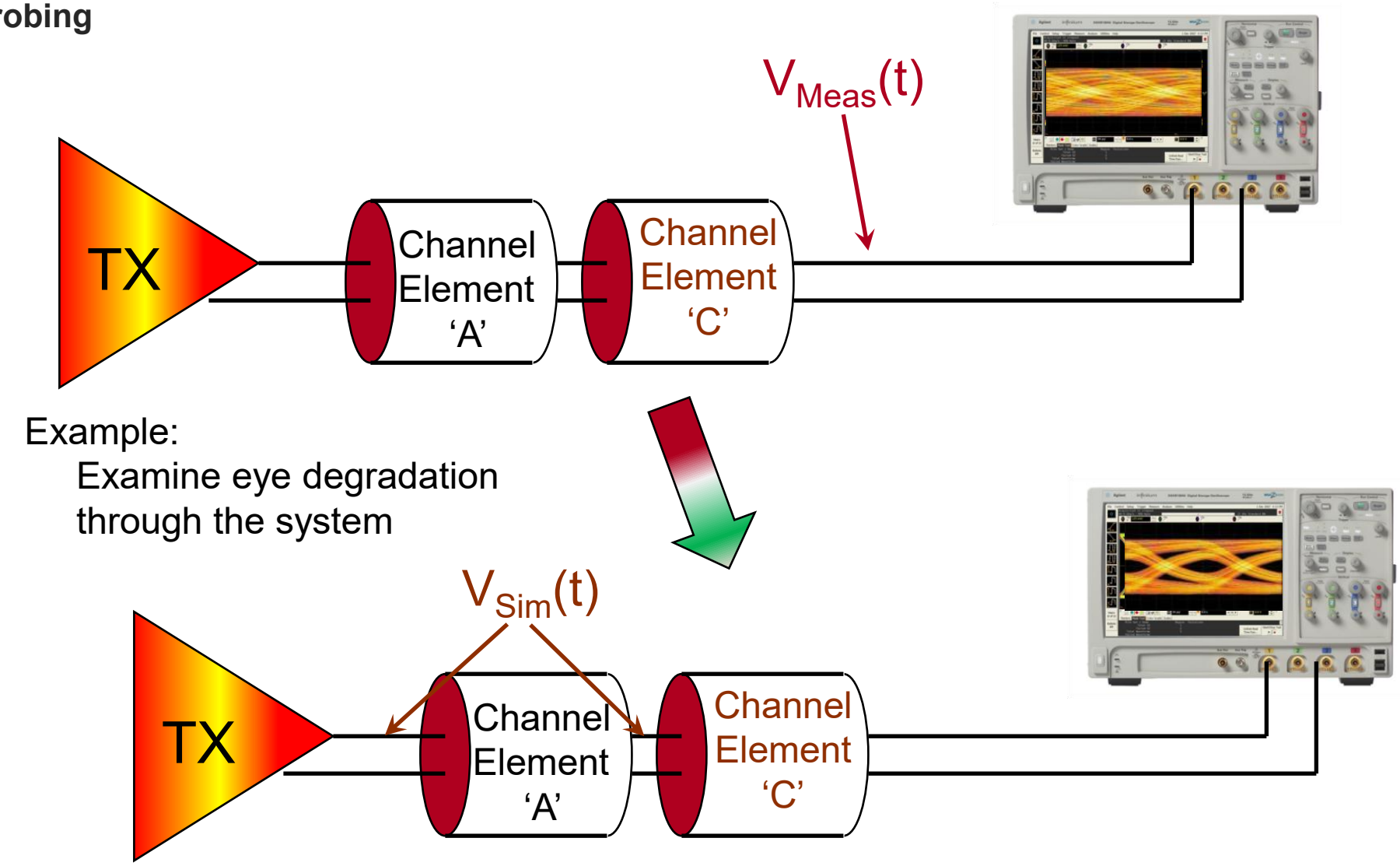
Example:

Replace a Test Fixture with a standard channel model.



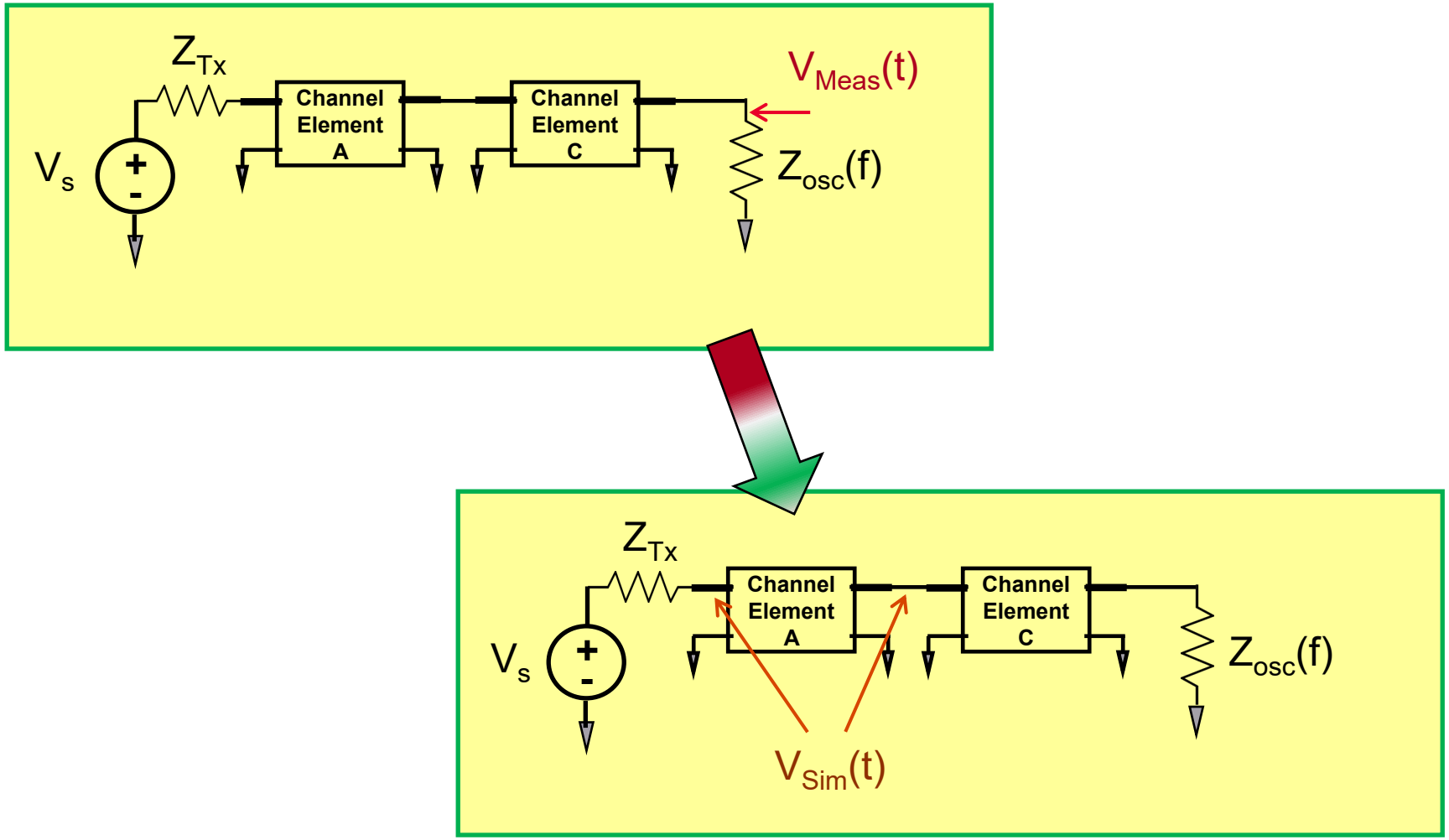
Relocating Observation Node

Virtual Probing

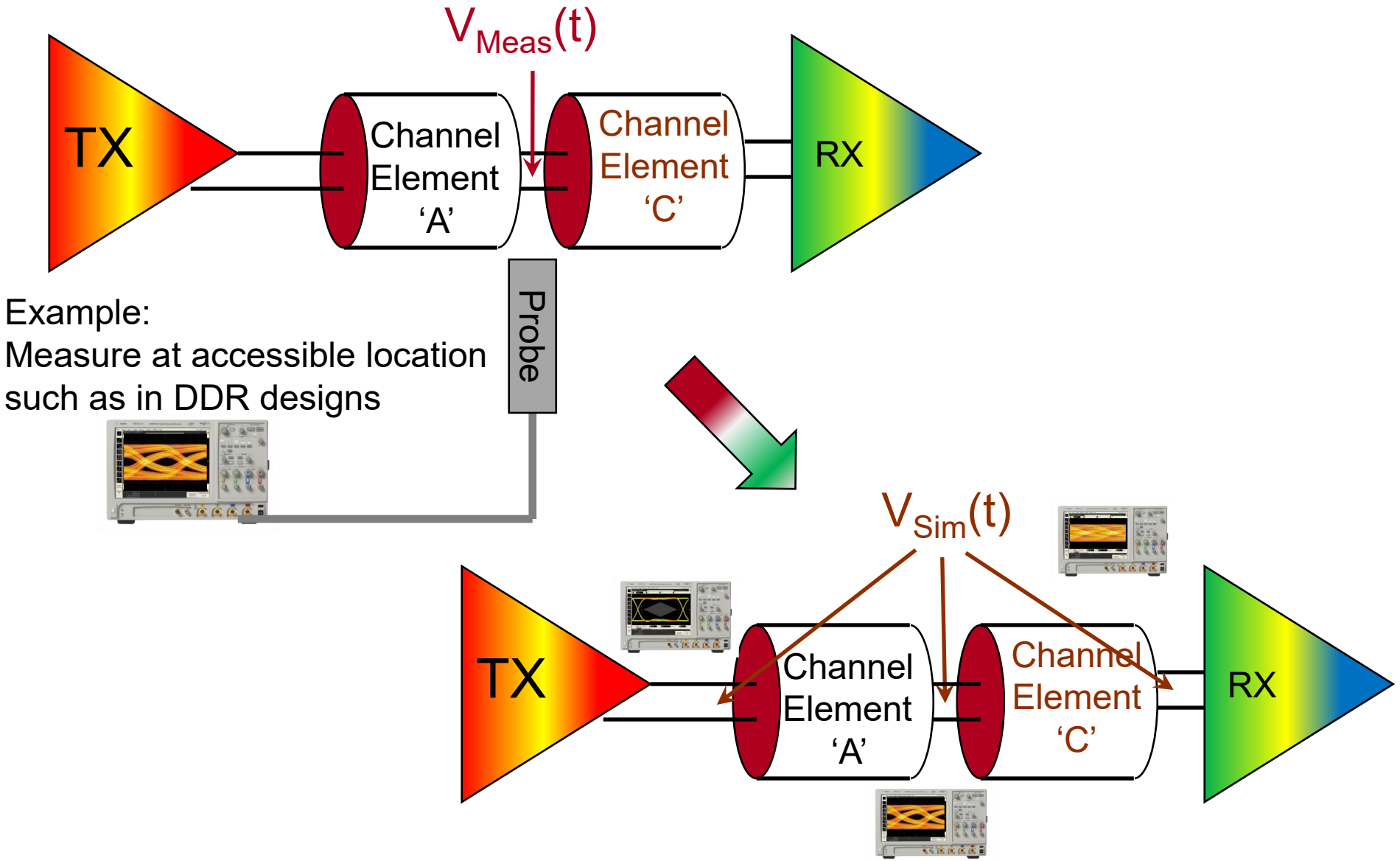


Relocating Observation Node

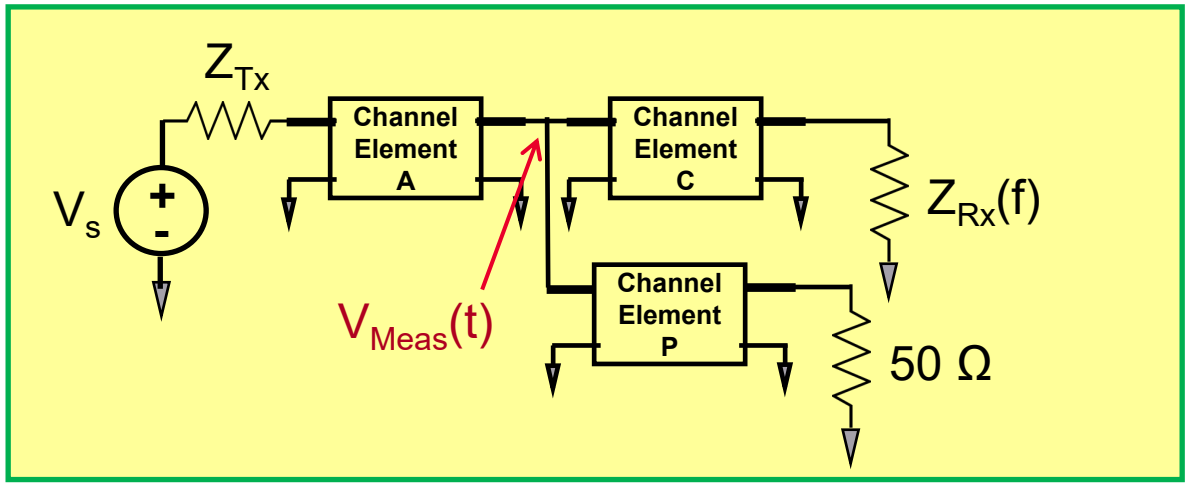
Virtual Probing

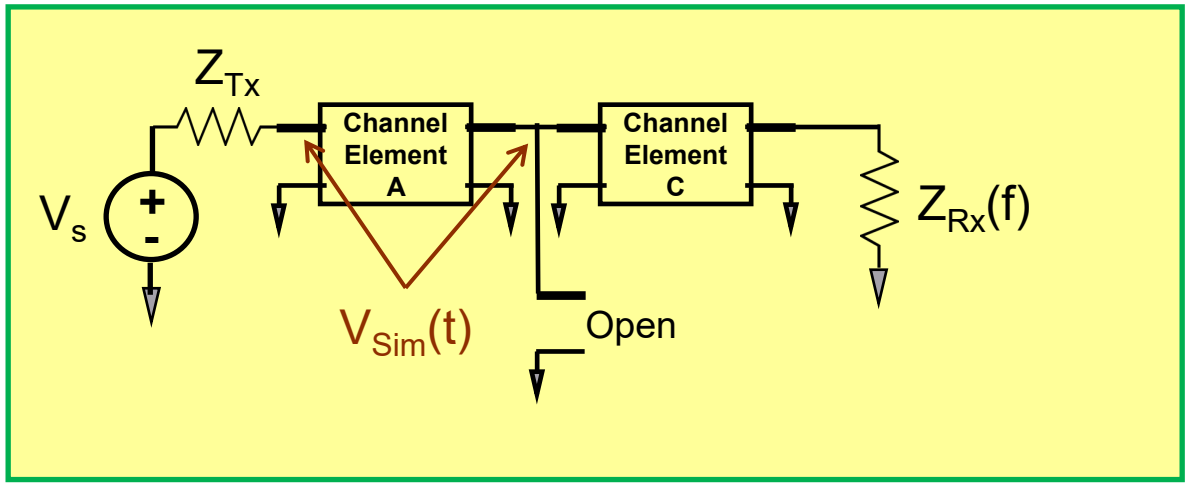


Removing the Effects of Probing

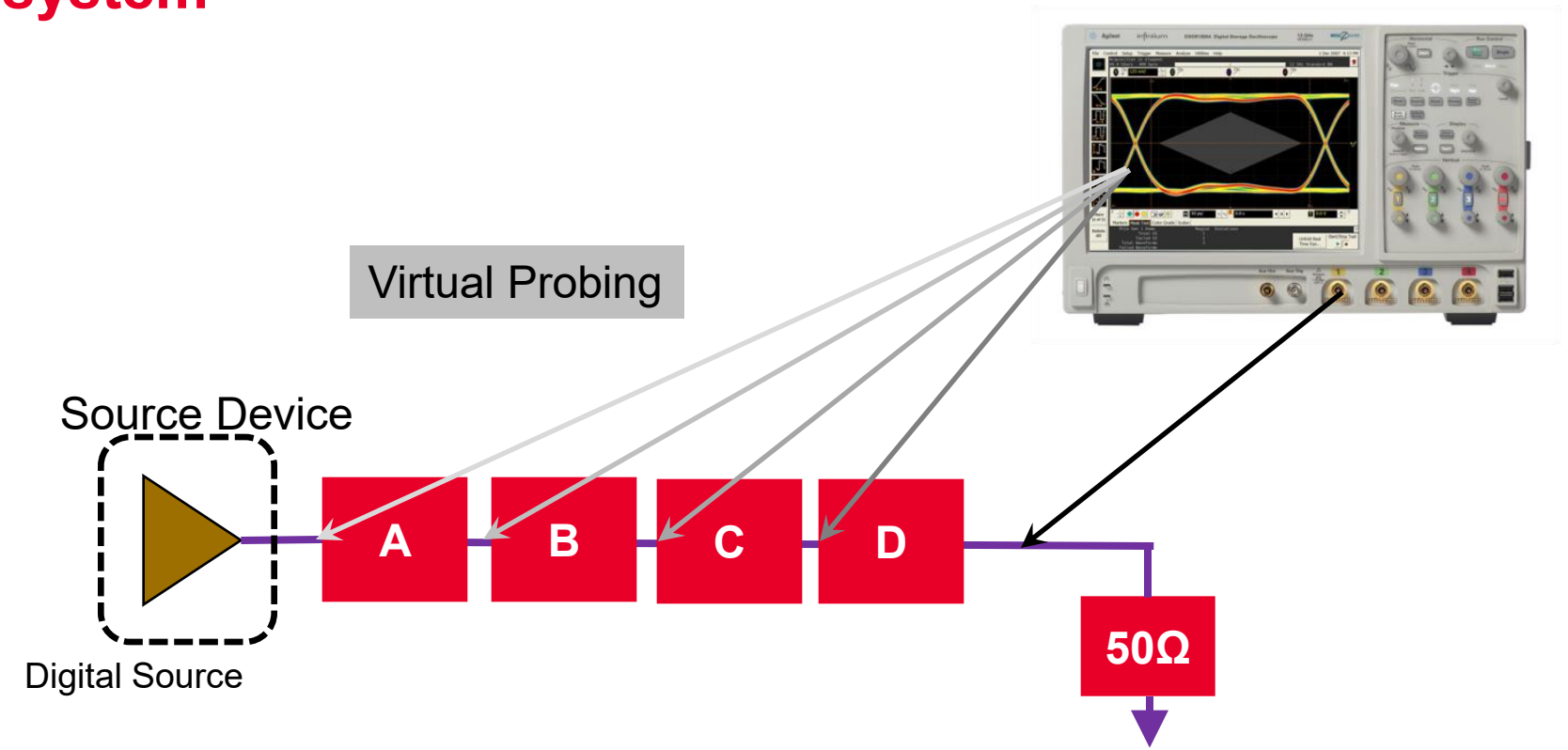


Removing the Effects of Probing



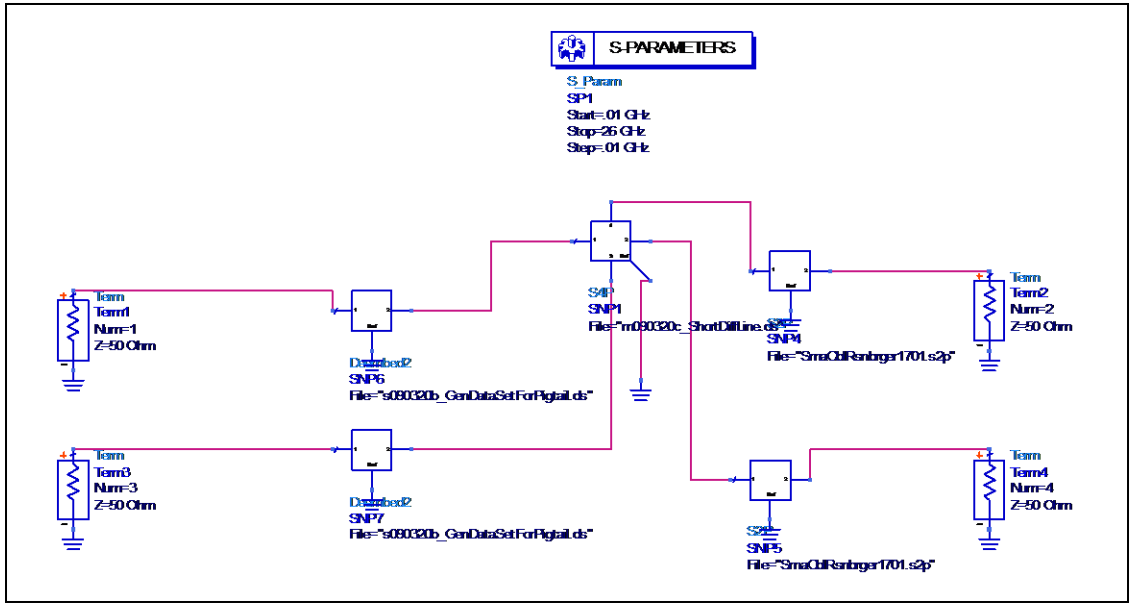


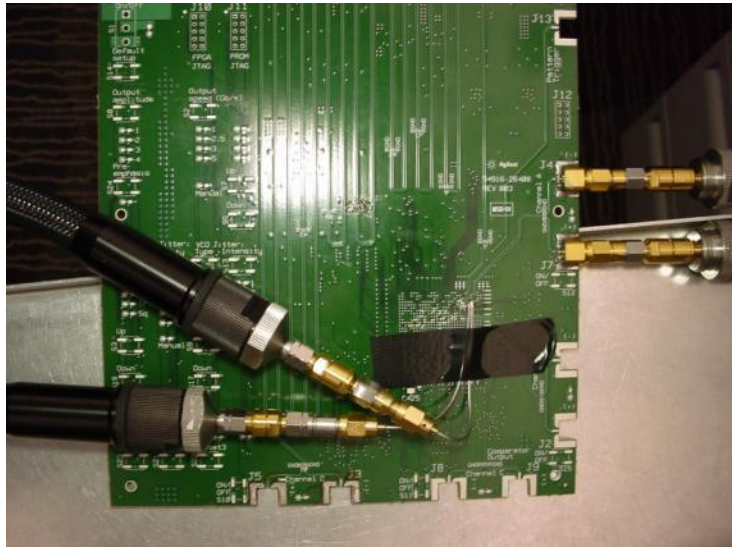
Modeling your system

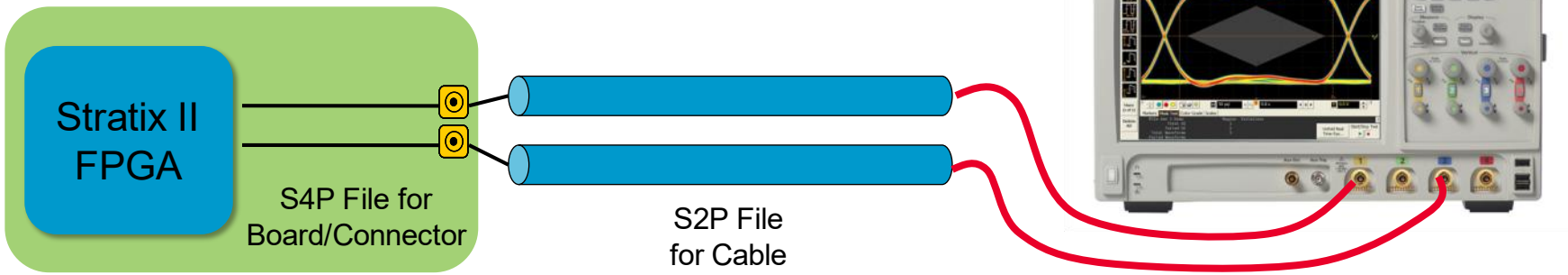


Circuit Elements: capacitors, inductors, resistors
Parameters: Z, Y, S-Parameters
Time Domain: Impulse Response
Frequency Domain: Transfer Functions

Creating models in ADS (Agilent Design System)







De-embedding the DDR2 BGA Probe

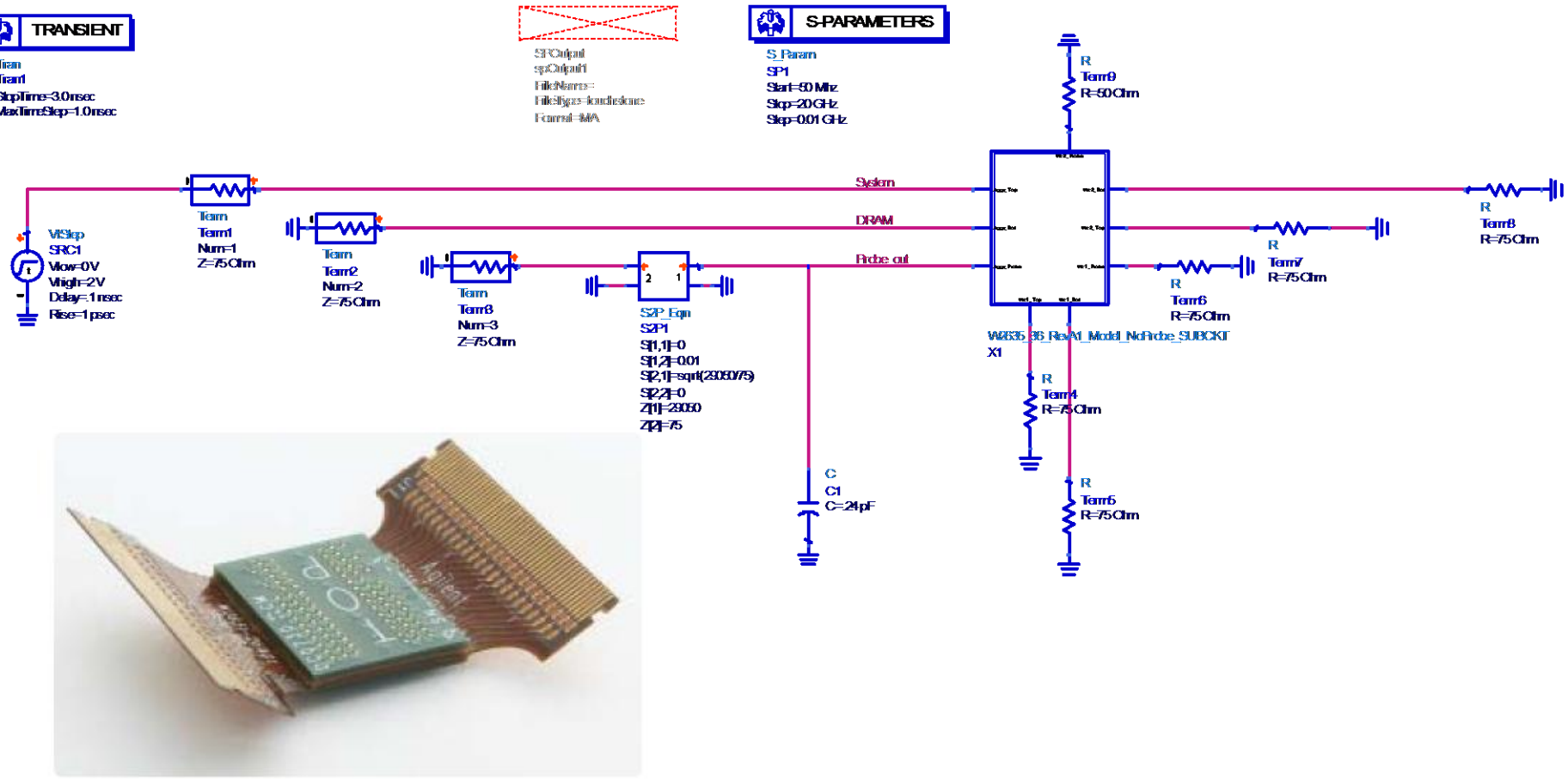
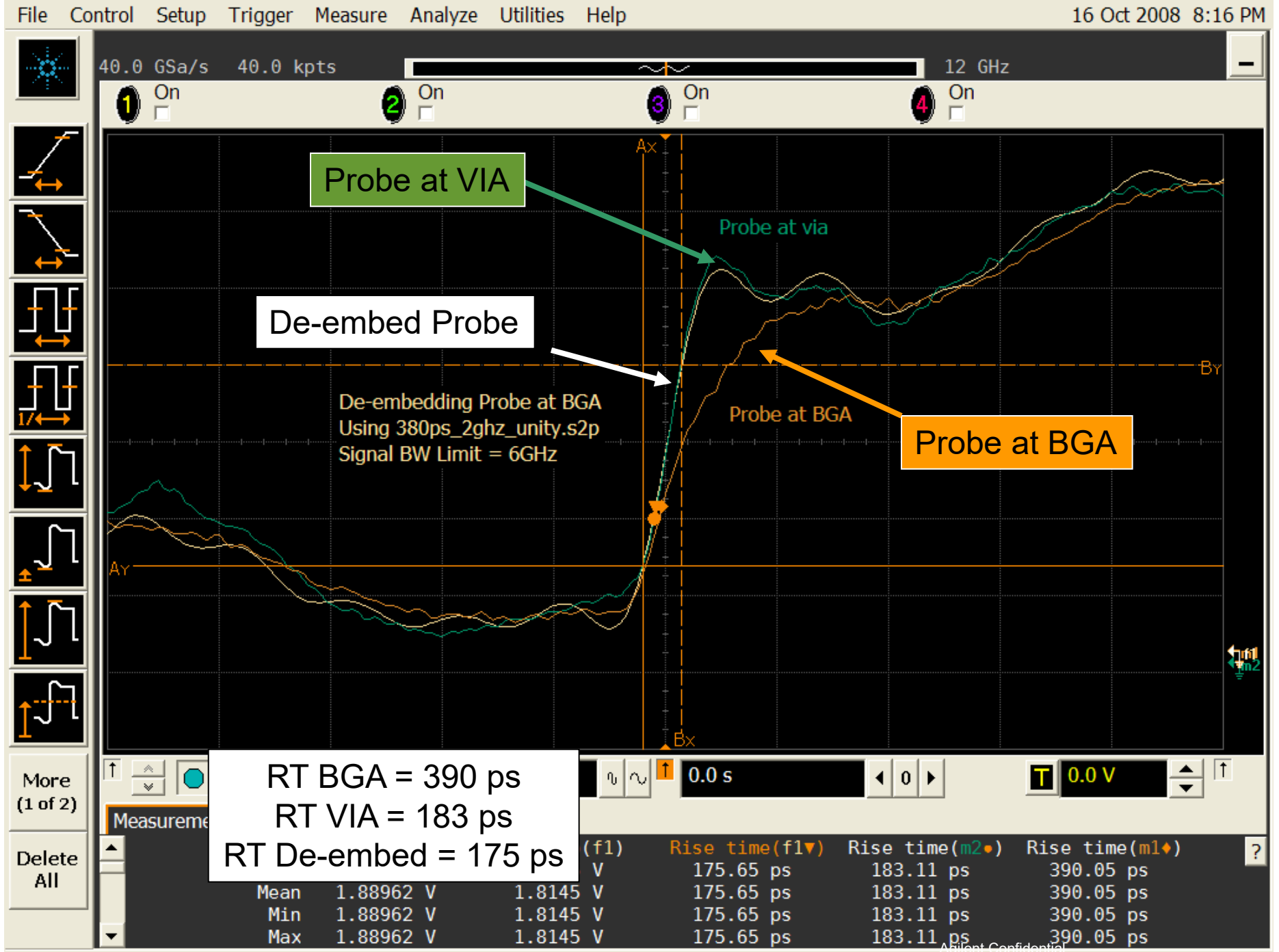


Figure 8. DDR2 BGA probe adapter for oscilloscopes and logic analyzers

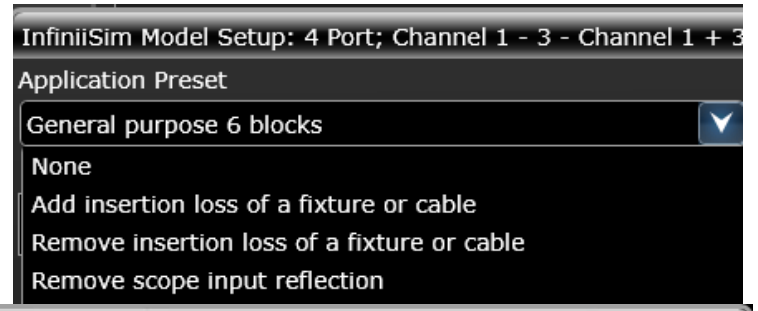


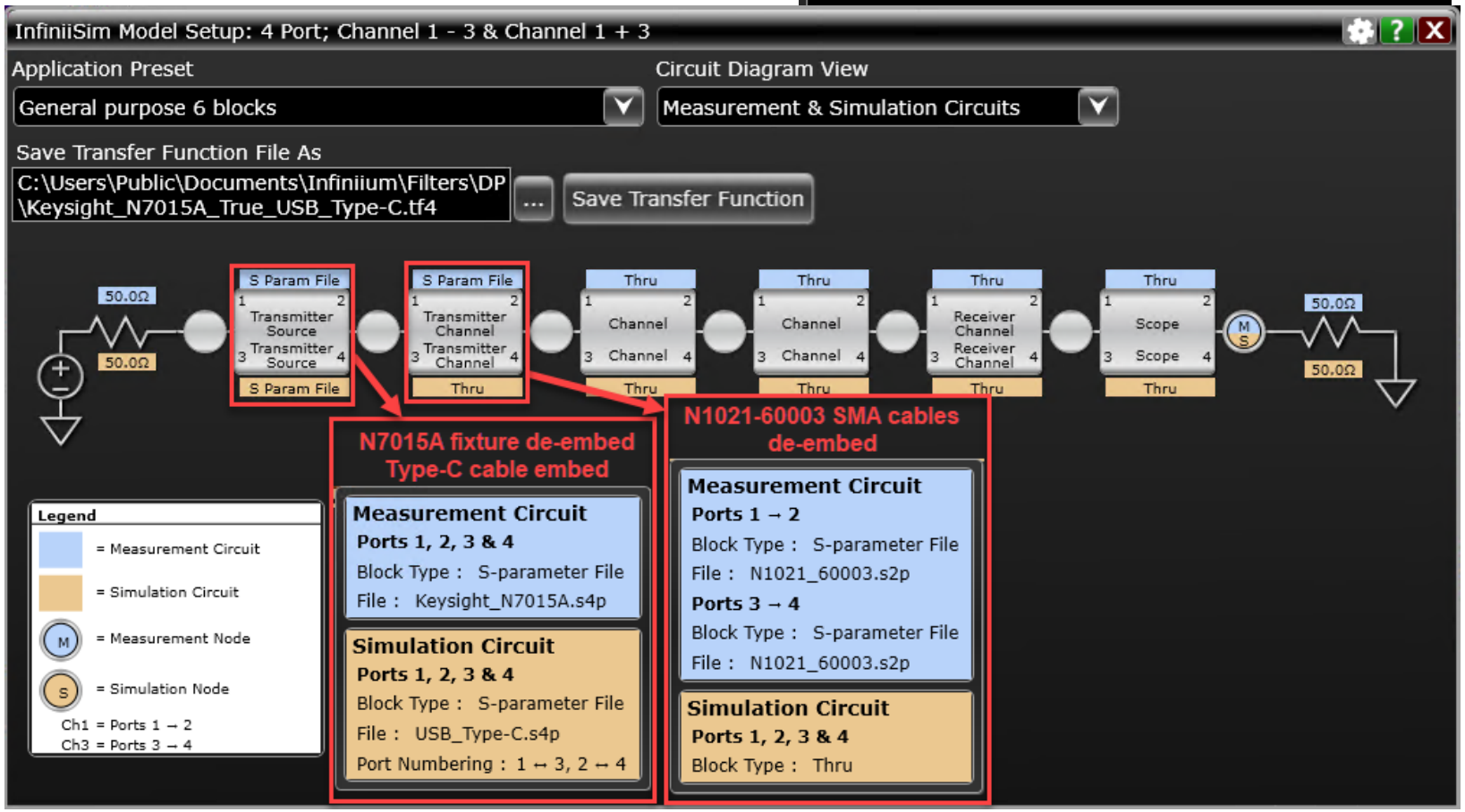
Agilent Confidential

Transmitter Testing

InfiniiSim – De-embedding and Embedding

- Embedding channel elements
- De-embedding channel elements
- DPoC use model
  - Embed a cable model
  - De-embed N7015A Type-C fixture
  - De-embed SMA cables
- InfiniiSim Basic
  - One “block” only
  - Insertion loss only (s21)
- InfiniiSim Advanced
  - Up to 9 blocks
  - Can use 4-port s-parameters
  - Many more options than Basic





Transmitter Testing

Equalization

- “Serial Data Equalization” (SDE)
- Opens eyes closed by lossy channels
- Three equalizer types
  - Continuous Time Linear Equalization (CTLE)
  - Feed Forward Equalization (FFE)
  - Decision Feedback Equalization (DFE)

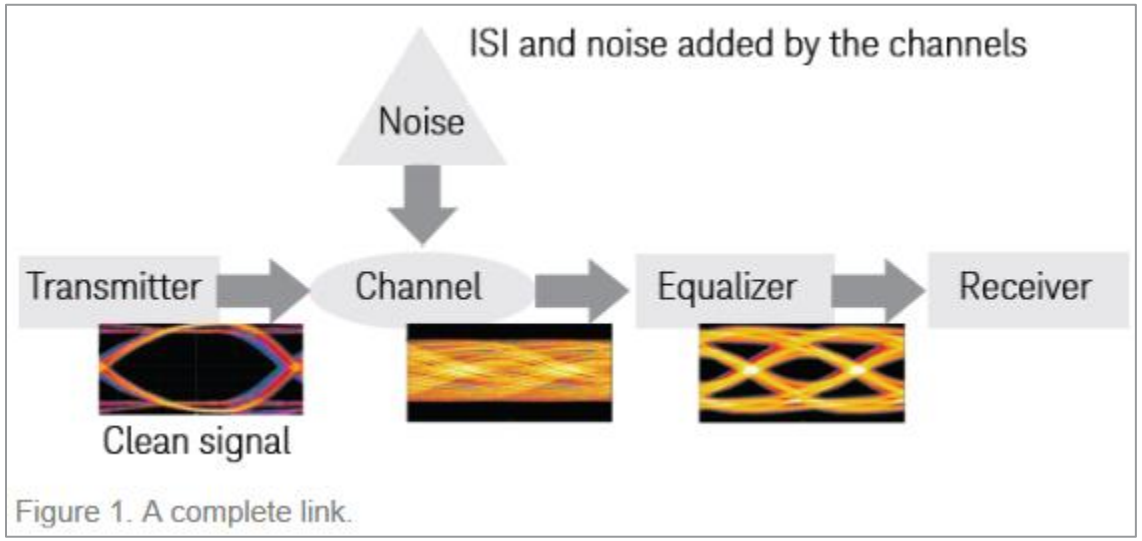


Figure 1. A complete link.

D9020ASIA

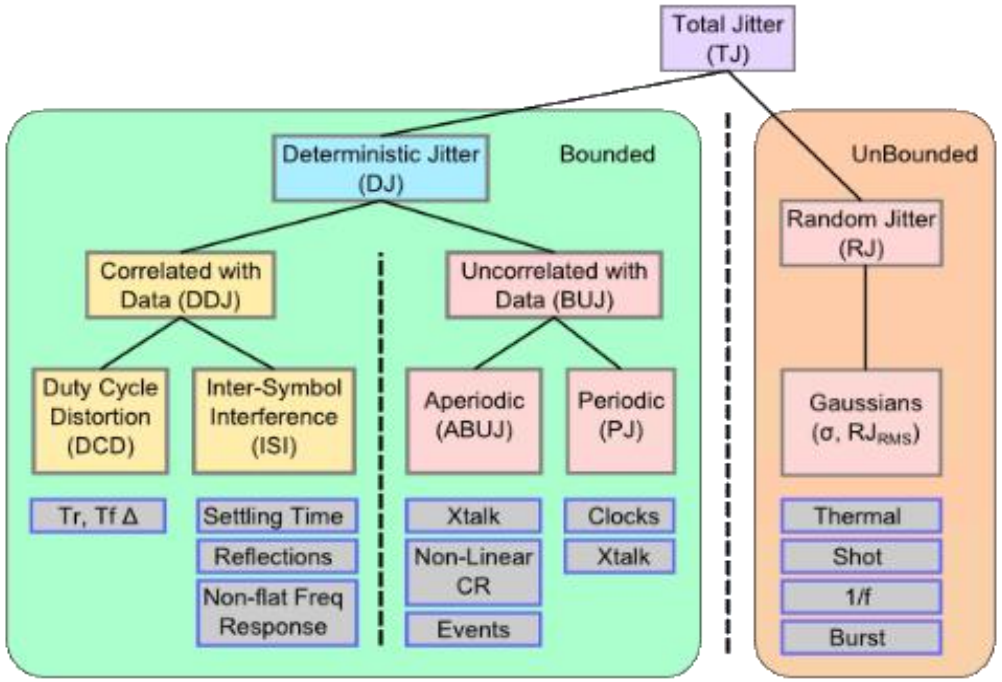
Advanced Signal Integrity Software for Infiniium Oscilloscopes

D9020ASIA is intended for any customer working in high speed digital applications where eyes are closed. Equalization, InfiniiSim, and Crosstalk/Power Integrity packages enable deep analysis as to why an eye is closed, and what it will take to open it. It is available on all Infiniium oscilloscopes.



Transmitter Testing

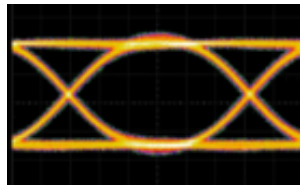
EZJit Complete – Jitter Analysis and Decomposition



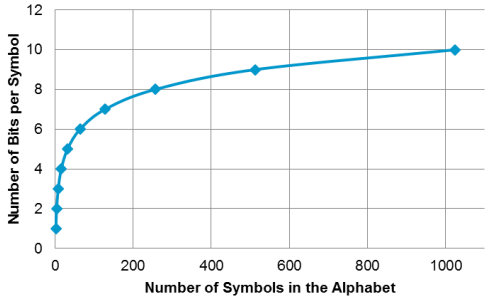


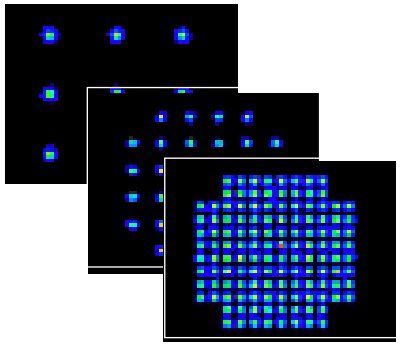
Applications and Their Requirements

BIG DATA DEMAND DRIVES TECHNOLOGY CHANGES

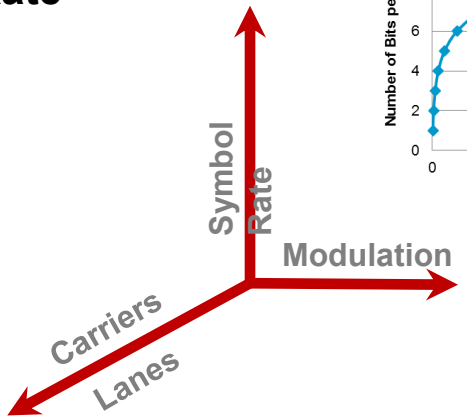


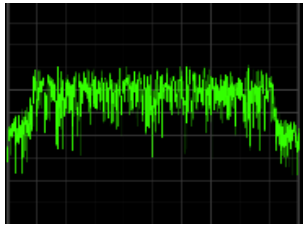
Increase Symbol Rate





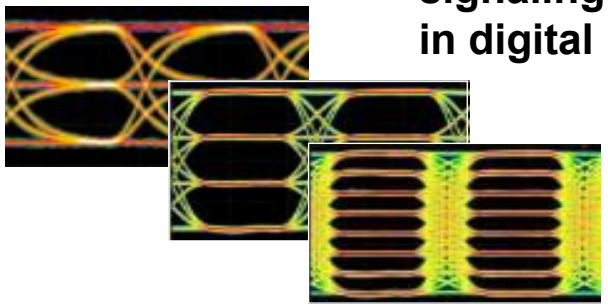
Maximize Bits per Symbol





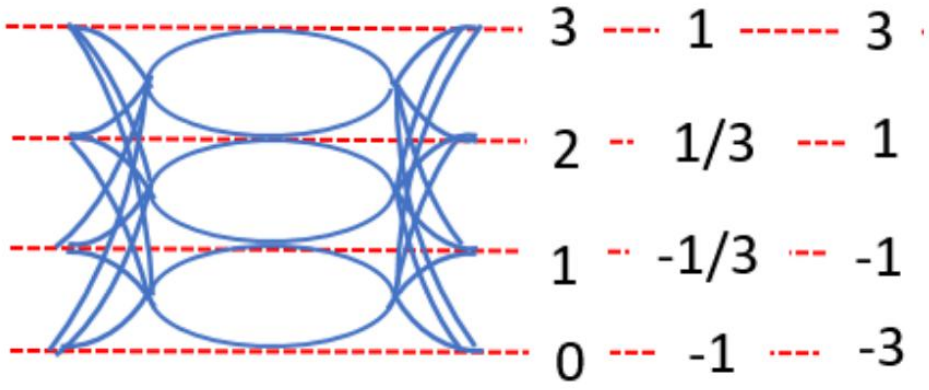
Maximize # of carriers

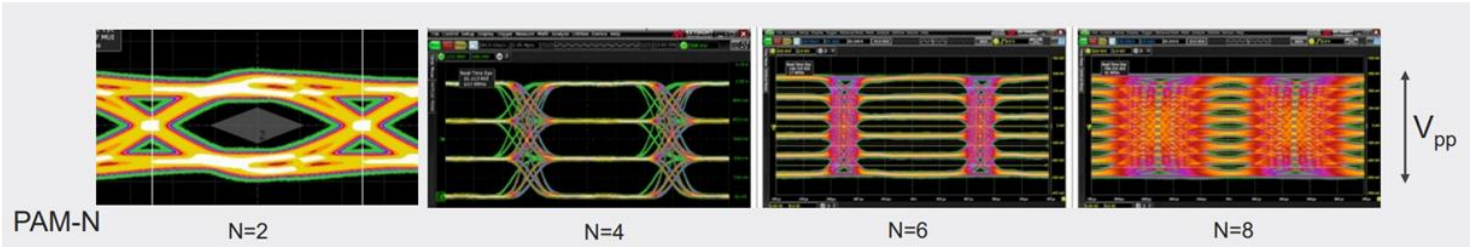
Multi level signaling in digital links,

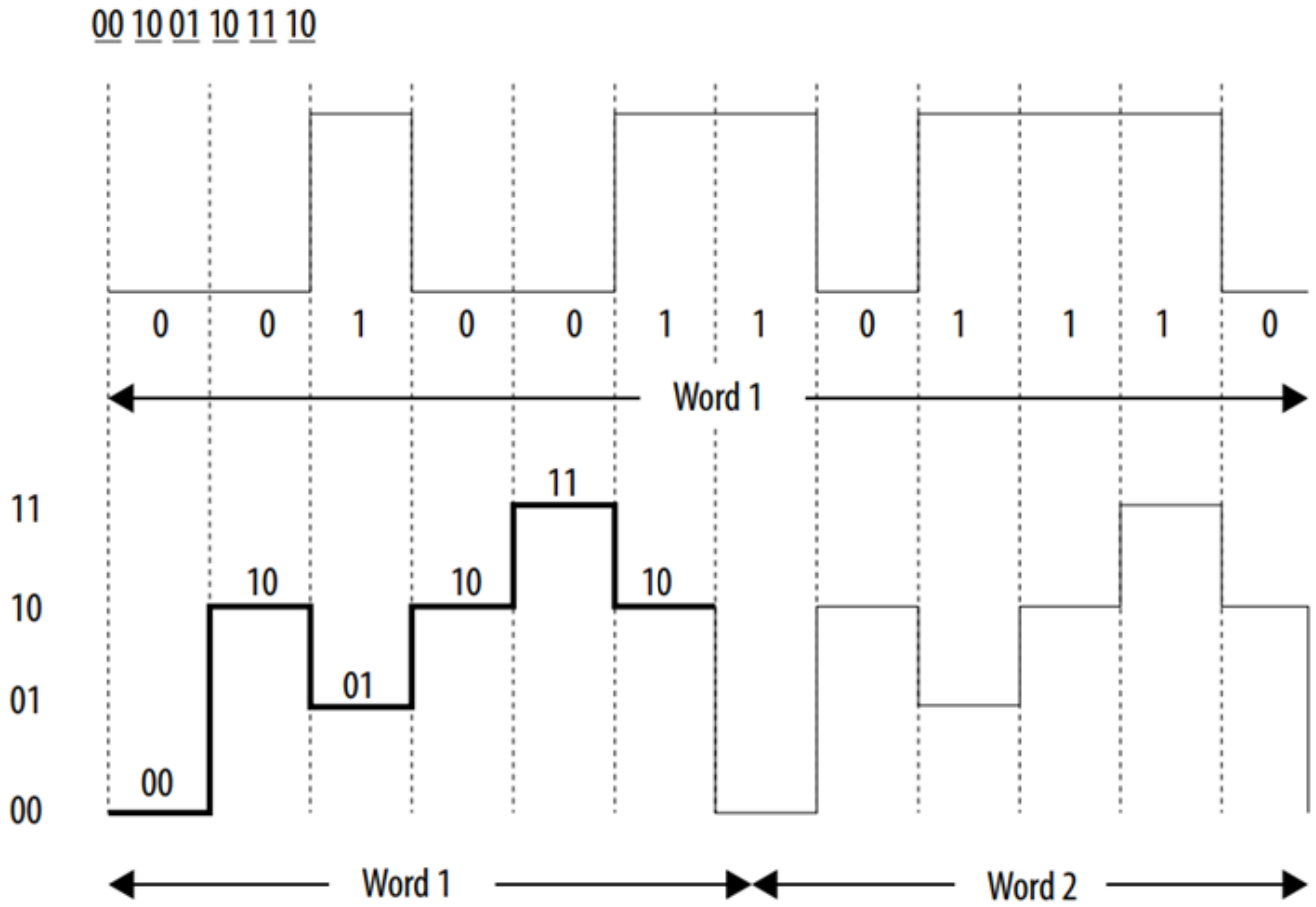


NRZ (PAM2) vs. PAM4 Coding

- 4 amplitude levels
- 2 bits per symbol – higher density of information
- Twice the throughput for the same baud rate
- Same Bitrate can be achieved for PAM4 running at half the symbol rate of an NRZ signal
- The PAM4 case is not gray encoded





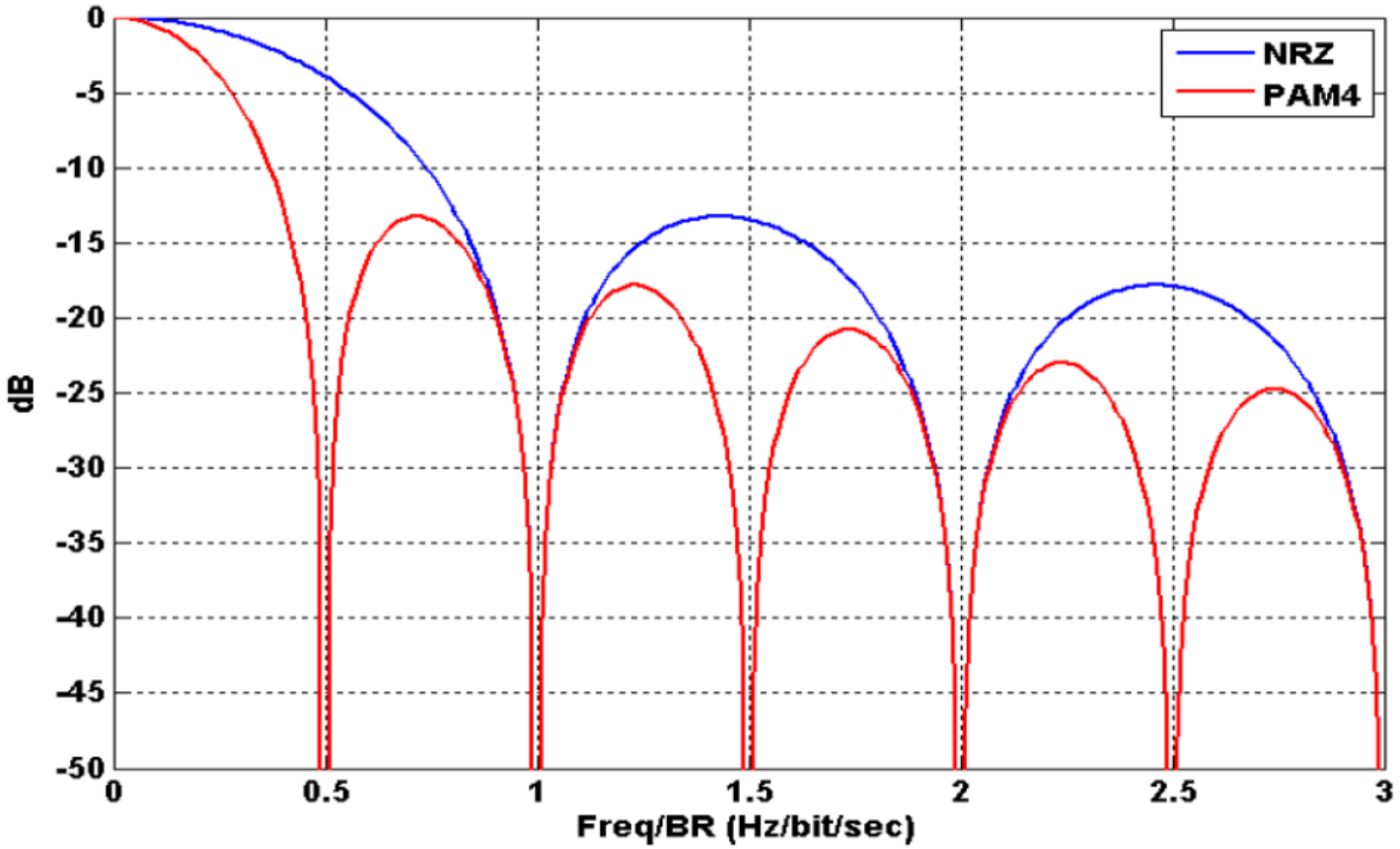


Intel AN 835: PAM4 Signaling Fundamentals, see: https://cdrdv2-public.intel.com/667071/an835-683852-667071.pdf

Power Spectrum Density of NRZ and PAM4

- At 56 Gbps, PAM4 requires half of the Nyquist frequency as that of NRZ.
- The SNR loss of a PAM4 signal compared to an NRZ signal is ~9.5 dB

$$\text{SNR loss} = 20 \times \log_{10}\frac{1}{3}$$



PAM4 $f_{Nyquist}$ = 56/4 = 14 GHz

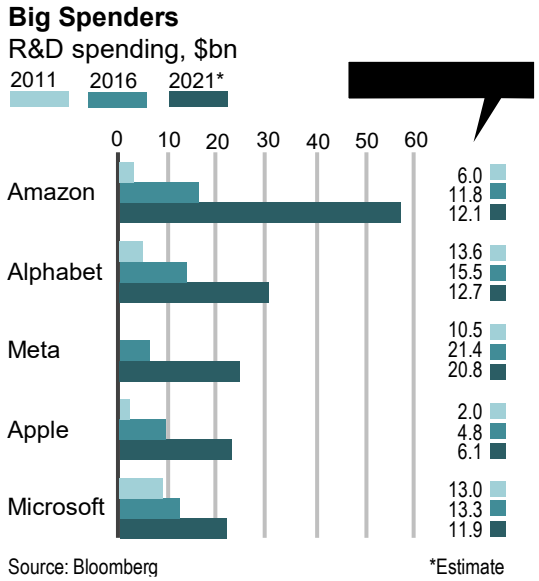
NRZ $f_{Nyquist}$ = 56/2 = 28 GHz

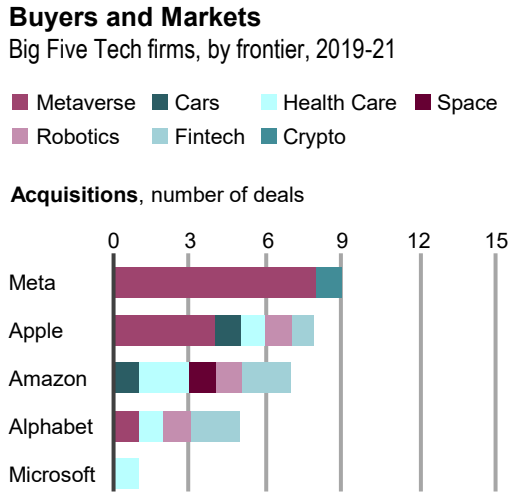
Intel AN 835: PAM4 Signaling Fundamentals, see: https://cdrdv2-public.intel.com/667071/an835-683852-667071.pdf

Why transition from NRZ to PAM-N?

AI - Business Driver for Data Centers

R&D spending from 9% to 12%
20% in „frontier technologies“





Acquisitions of know deal size >50bn
>25% of deals AI related

AI-platforms	Increasing workloads	• Faster silicon/reduced node size • Compute disaggregation • Higher integration • Move compute to the edge	• 4nm, 3nm, 20A, 18A… • High-speed I/O, PCIe, CXL • CPO, UCIe, optical I/O • LLM vs. medium small LM

Cloud Service Provider: Microsoft, Google, amazon, Meta, Alibaba.com

NEM/OEM: cisco, ciena, Juniper Networks, DELL Technologies, NOKIA, hp

Optical Transceiver: eoptolink, CIG, INNO LIGHT, Accelink

Optical Component: FUJITSU Fujitsu Optical Components, Sumitomo Corporation, LUMENTUM, COHERENT

Chip: intel, NVIDIA, AMD, SAMSUNG, BROADCOM, MARVELL

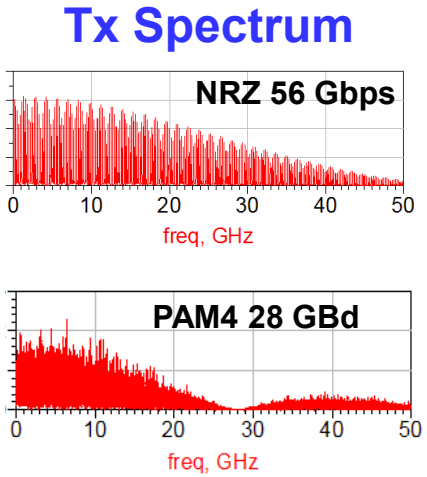
IP: SYNOPSYS, cadence, ALPHAWAVE SEMI

Research: Columbia University, KIT, ETRI, University of Southampton

Why Does the Industry use PAM4?



- NRZ > 28 Gb/s limits trace length or increases cost due to more expensive PCB material
- PAM4 yields 2 bits / symbol
  - ✓ Effectively halves the channel BW needs
- Enables designers to develop products that meet the cost structure and are based on mature 100G optical components.



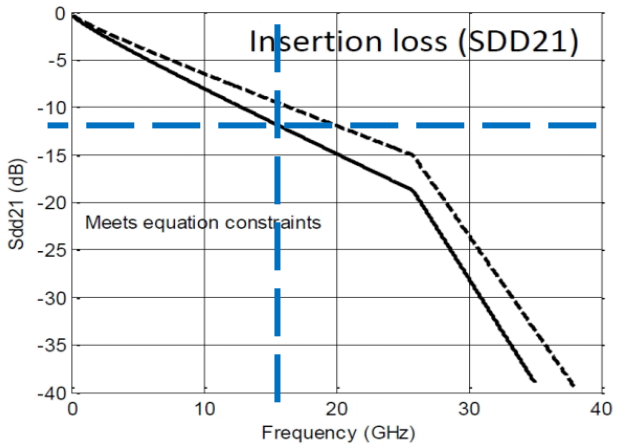
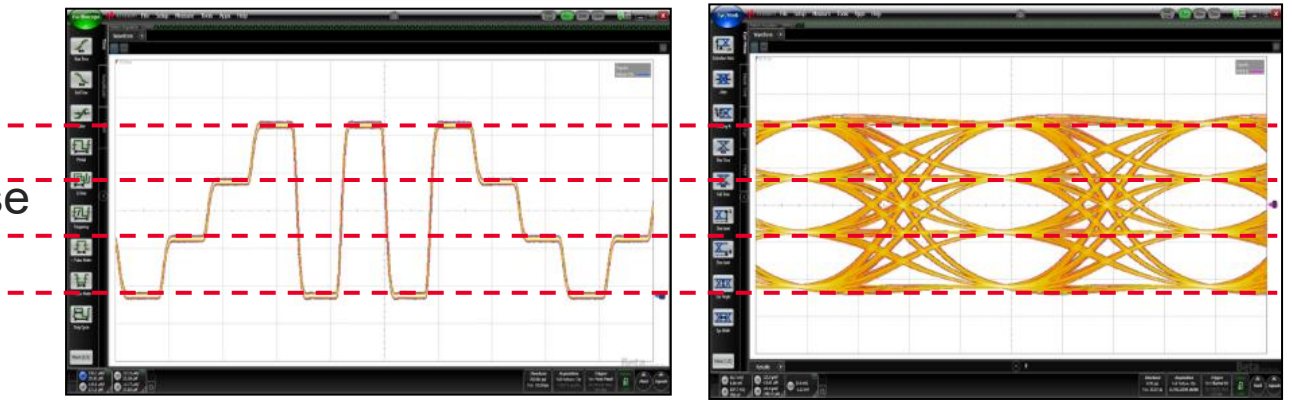


Figure 5: CEI-56G VSR NRZ channel

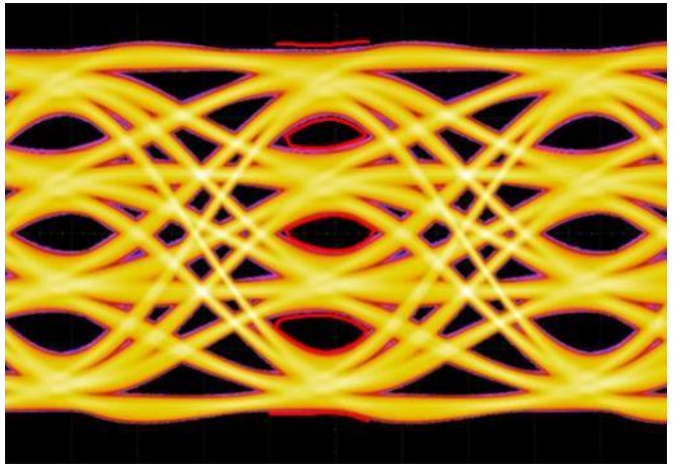
+ PAM4: Pulse Amplitude Modulation 4-level
+ 2 bits of information in every symbol
  - ✓ ~ 2x throughput for the same baud rate
  - ✓ 26.56 GBd PAM4 = 53.125 Gb/s
- Higher SNR requirement, more susceptible to noise → 3 eyes vs. 1 eye → **FEC essential**
- More complex PHY Chip design, linear TIA and RF driver Amp



Challenges Moving From NRZ to PAM4

Design and Measurement

- Increased receiver sensitivity requirement
  - Packing 4 levels into amplitude swing of 2 – lose 9.6 dB SNR
  - It is not just about timing jitter budgets anymore!
  - Need better management of noise and return loss
- Finite rise time creates inherent DDJ – Tighter jitter requirement!
- How to implement clock recovery?
- FEC often required due to more closed eyes with lower SNR
- How is mask testing done on such an eye diagram? Or what replaces eye mask testing?
- What are the implications of using FEC on how components and systems are tested?....



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Why Not Just Adapt NRZ Methods to PAM4?

In some cases it works, and in others it doesn't

- Extinction ratio and OMA for PAM4
  - NOT measured on the aggregated PAM4 eye diagram
  - Measured on the zero level and the three level
  - Measured on specific bit sequences, so the scope MUST be pattern locked
    - Long patterns like PRBS31 are no longer allowed (PRBSQ13 and SSPRQ are used)
- New measurement names to distinguish PAM4 method
  - Outer OMA
  - Outer Extinction ratio

power level P_3, measured over the central 2 UI of the run of 7 threes, and the average optical launch power level P_0, measured over the central 2 UI of the run of 6 zeros, as shown in Figure 122–3.

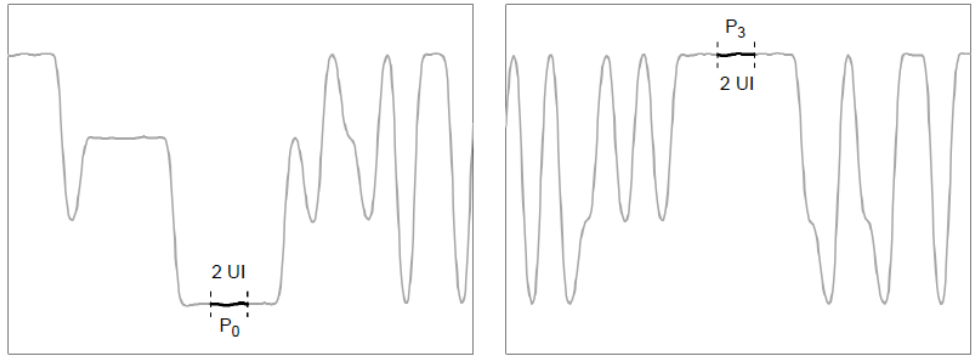
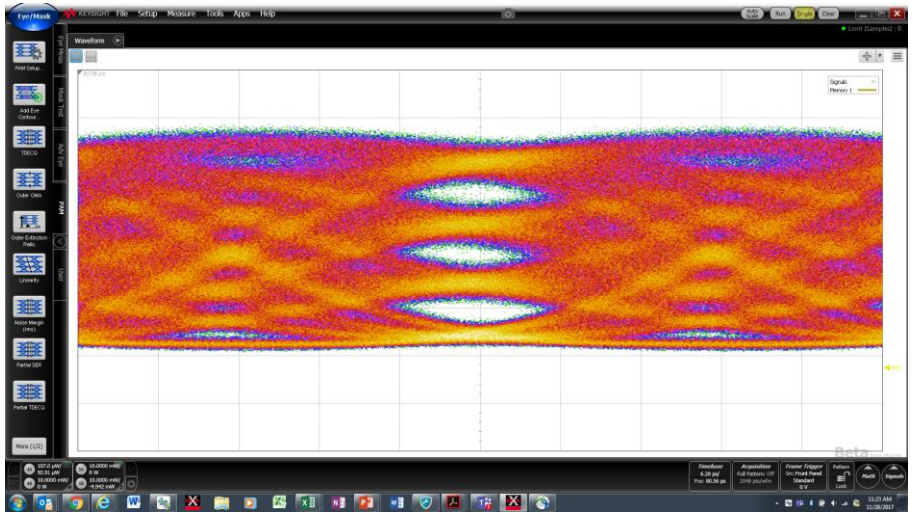


Figure 122–3—Power levels P_0 and P_3 from PRBS13Q test pattern

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Why did we drop the eye-mask test????

- Eye closure is expected to be severe, requiring receiver equalization, reducing the value of an eye mask
- It is certainly possible to have a PAM4 eye-mask, but the standards committee felt that it would not be a very good predictor of performance in an actual system
- Emphasis was placed on the transmitter dispersion measurement, as with both NRZ and PAM4 it is a better predictor of system level performance



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TDECQ

Transmitter Dispersion and Eye Closure Quaternary

- Tells you the performance of your transmitter relative to an ideal transmitter
- For NRZ TDP (Transmitter Dispersion Penalty), we literally measured the BER performance of the transmitter compared to an actual golden transmitter
  - How much extra power was required at the receiver to compensate for non-ideal performance

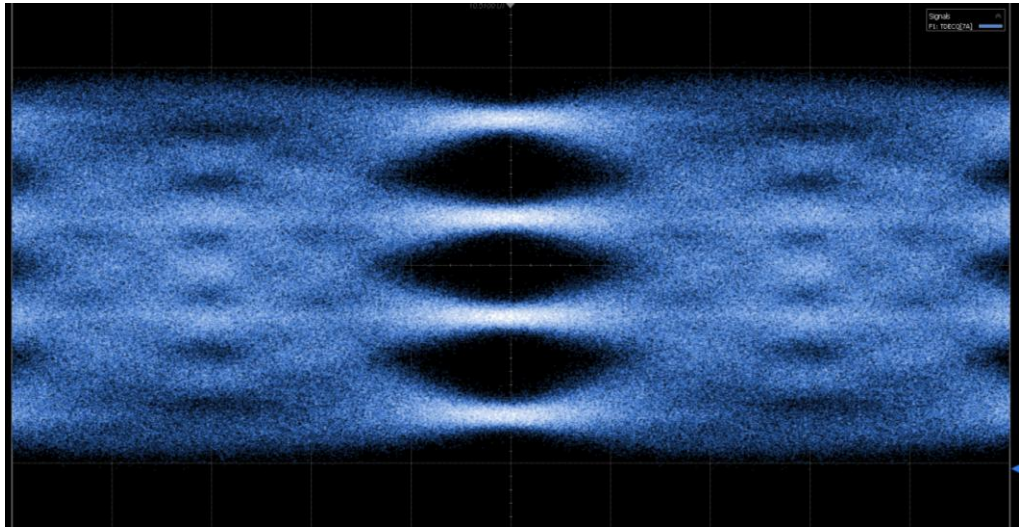
- For TDECQ we indirectly measure SER (symbol error ratio)
  - The transmitter metric is easily applied to the overall link budget

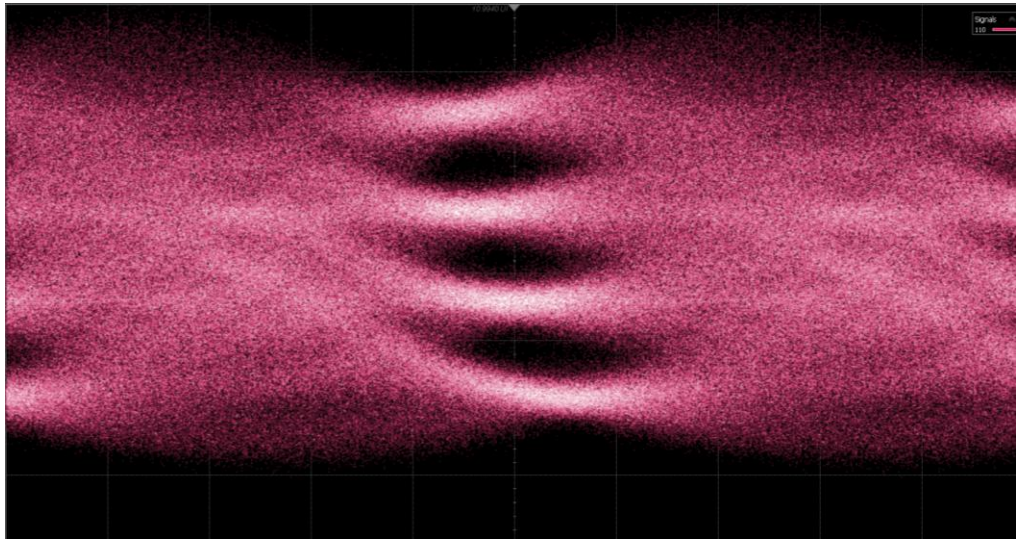
© 2018 Keysight Technologies

What defines a good transmitter?

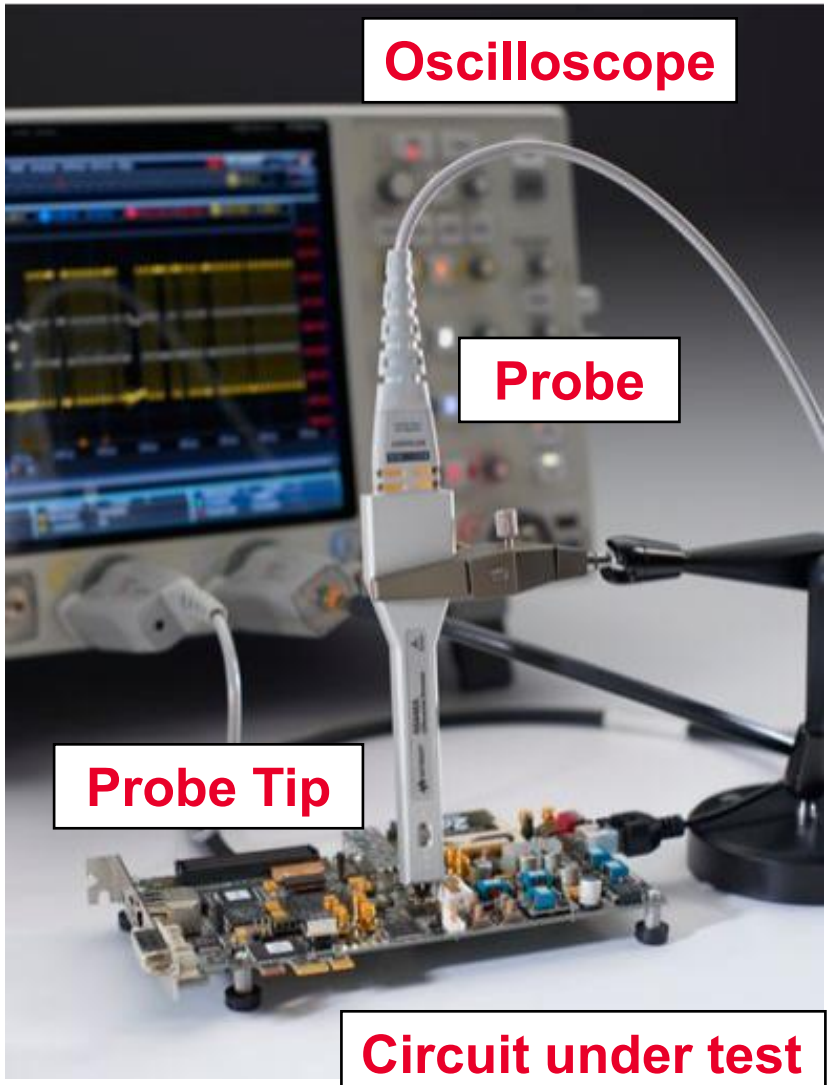
- Obviously, the blue waveform is better than the red
- How much better?
- Could both achieve a working optical link?

- Combined with transmitter power and waveform quality an optical system designer needs to consider several things including:
  - Channel loss and dispersion
  - Receiver sensitivity





Probing Affects Your Measurement

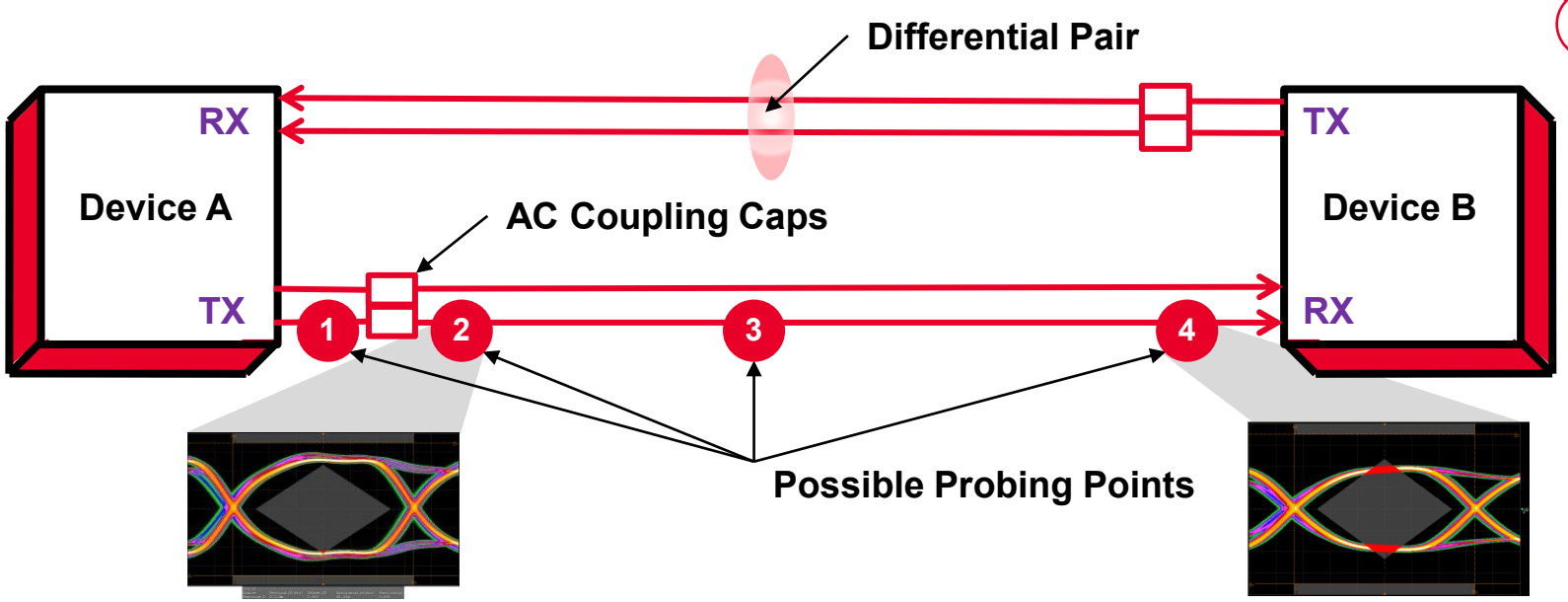


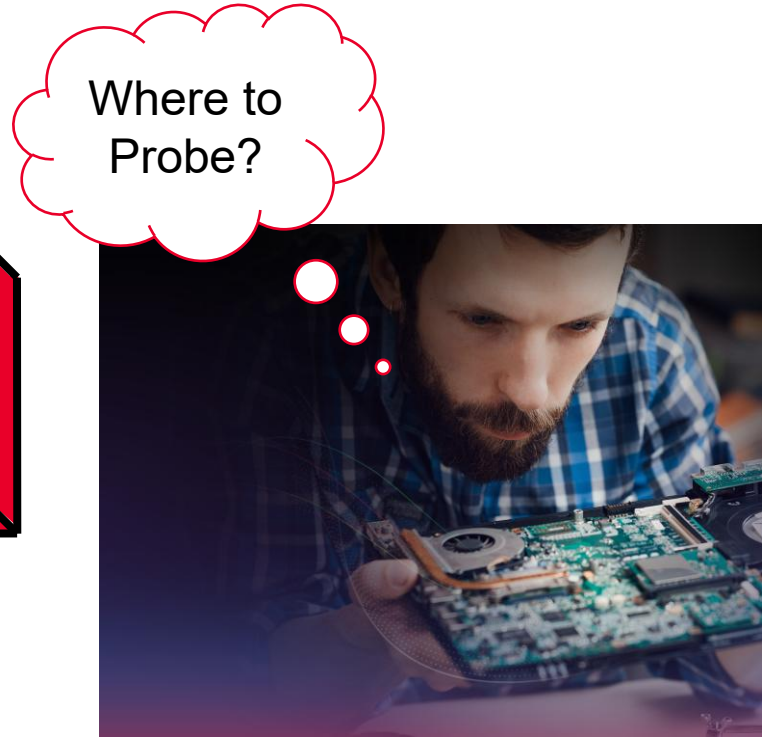
The electrical behavior of your probe affects both your measurement results and the operation of your circuitry. Taking action to ensure these effects are within acceptable limits is a key step to successful measurements.

Key Considerations when Probing:

- A probe with a probe tip and an oscilloscope are included in the overall system response, thus affecting the measurement bandwidth and the frequency response itself.
- Connecting a probe to your DUT/circuit can directly change the response of the DUT because of loading effects.

Where You Probe Matters



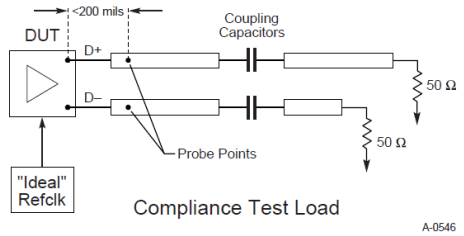


Probing Point	Location	Good?	Comments
1	TX side of coupling capacitor	It depends	Depends on what you want to measure. Will show more TX characteristics.
2	Channel side of coupling cap near TX	Yes	Removes DC component from TX. Second best option.
3	Mid-Bus	No	Denotes a short channel which is reflection dominated. Worst of all points to measure.
4	RX side (Far End)	Yes	Closest point to RX. Decoupled from transmission line. **The best option**

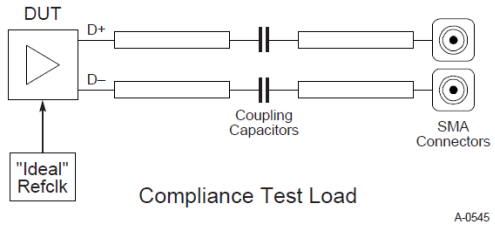
Refer to Standard's Specification to Define Test Points

3 examples with 3 different approaches

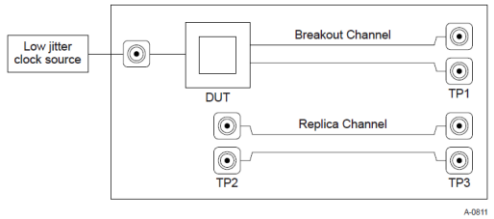
- **PCI Express Base (PCI- SIG):**



Required Setup for Characterizing a 5.0 GT/s Transmitter

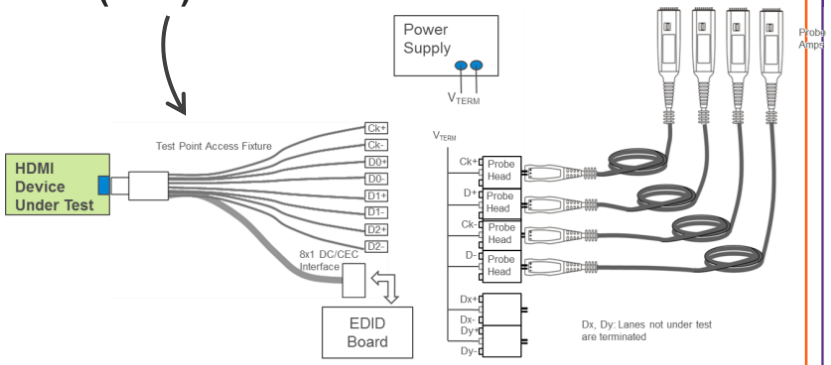


Allowable Setup for Characterizing a 2.5 GT/s Transmitter

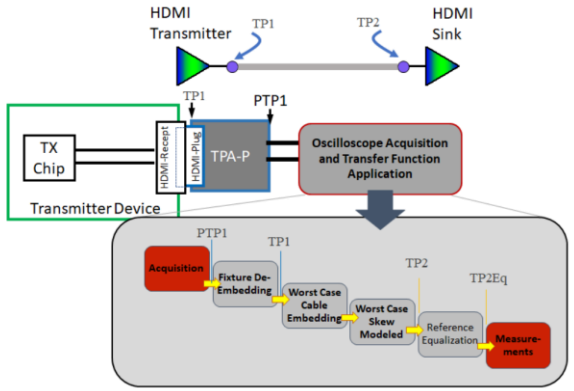


Tx Test Board for Non-Embedded Refclk for PCIe 5.0

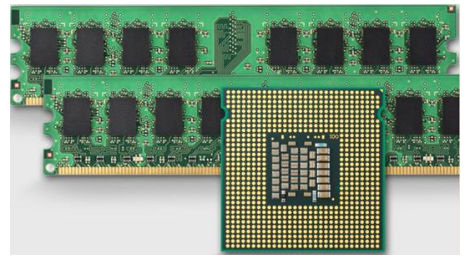
- **HDMI 2.1 (HDMI Forum):**
  - You need to use a **Test Point Adapter (TPA)** or Test fixture:



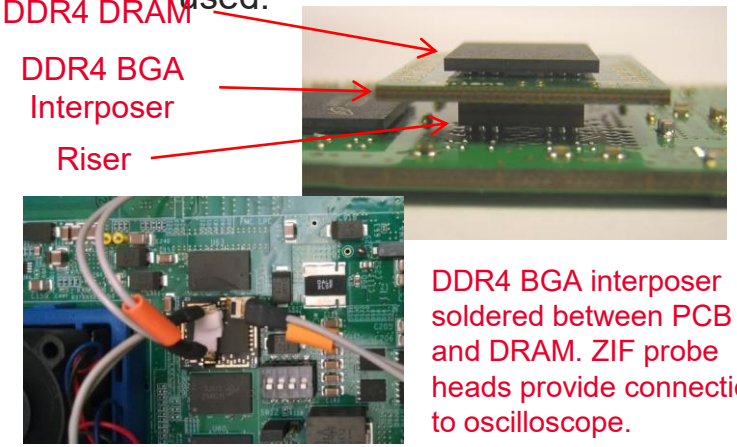
  - **Different test points** are defined for different tests:



- **(LP)DDRx DRAMs (JEDEC):**
  - Electrical Characteristics and AC Timing are defined **on DRAM balls**.



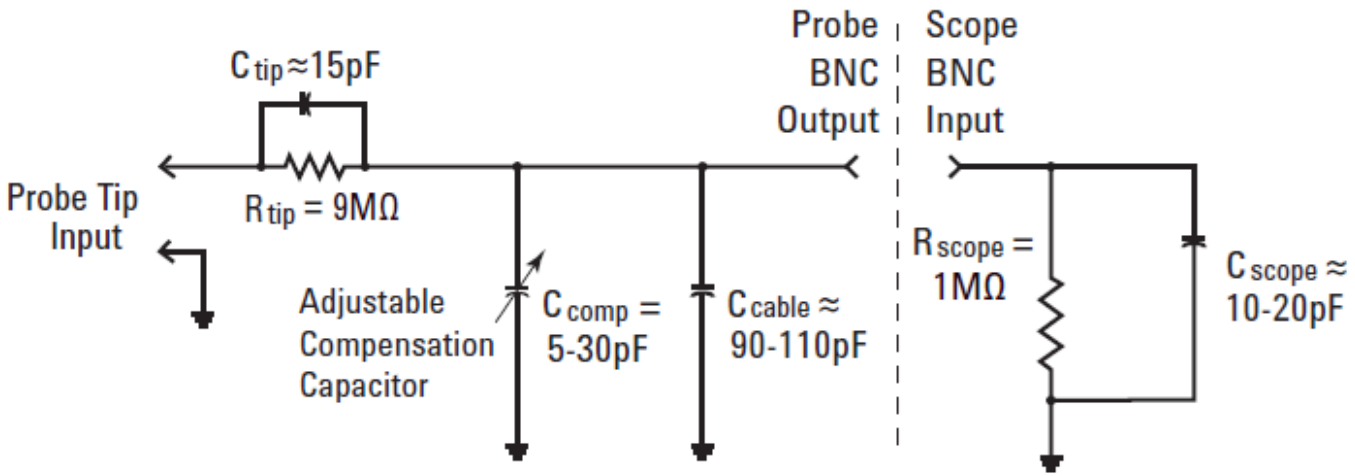
  - There is no possibility to connect to balls but **interposer approach** can be used:



DDR4 BGA interposer soldered between PCB and DRAM. ZIF probe heads provide connection to oscilloscope.

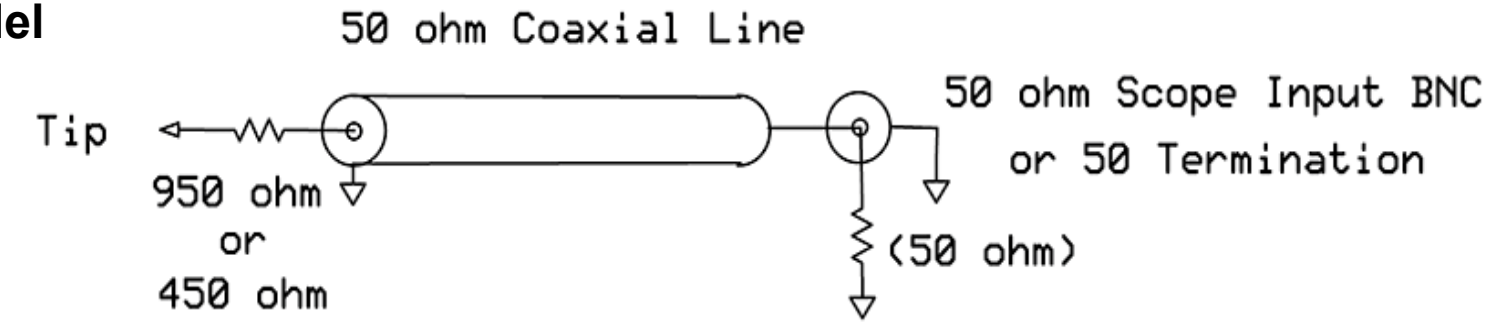
Passive or Active Probe?

What to choose for your measurement



- Capacitors act as open circuits at low frequency.
- Inductors act as short circuits at low frequency.
- Simplifies to a 9-MΩ resistor in series with the scope's 1-MΩ input termination.

Passive 10:1 Probe Model

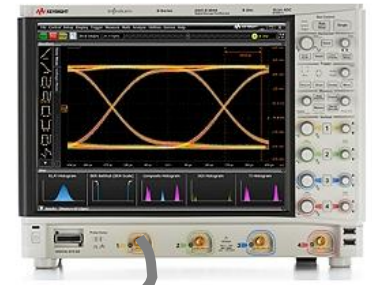


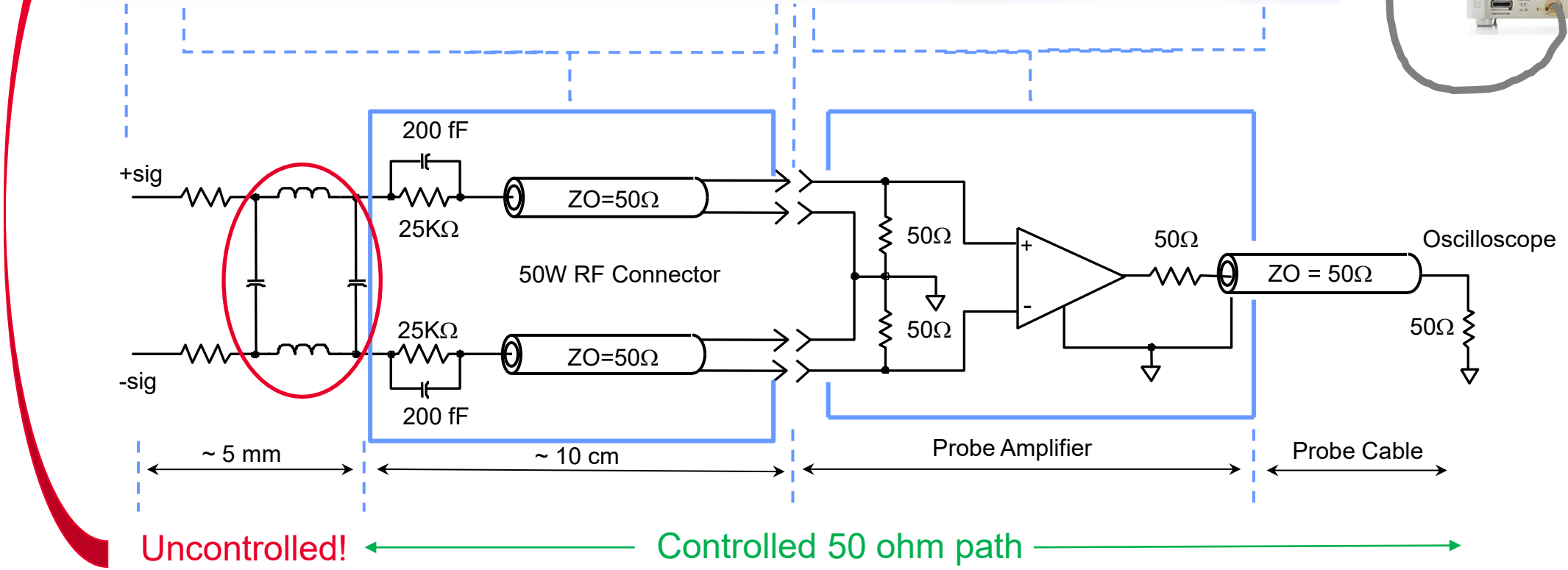
Lo-Z Resistive Passive Probe

InfiniiMax I/II Probe Architecture

This uncontrolled ~4 mm tip leads may have a huge effect on the performance of your probe and the entire measurement system







Varying Lead Length/Span Affects Probe Bandwidth

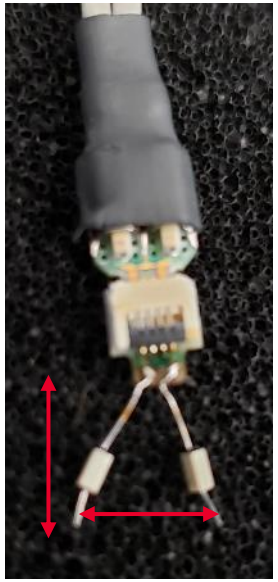
InfiniiMax II N5425B ZIF head + N5426A ZIF tips or N5451A Long-wire ZIF tips



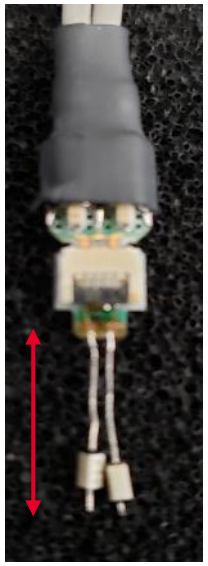
2mm, 12.3 GHz



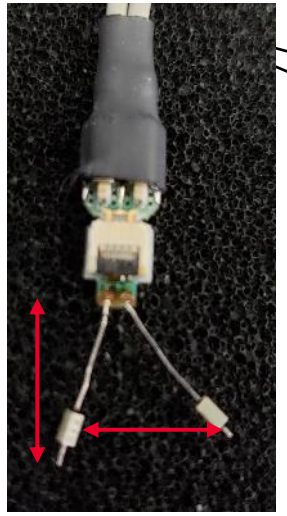
7mm, 9.9 GHz



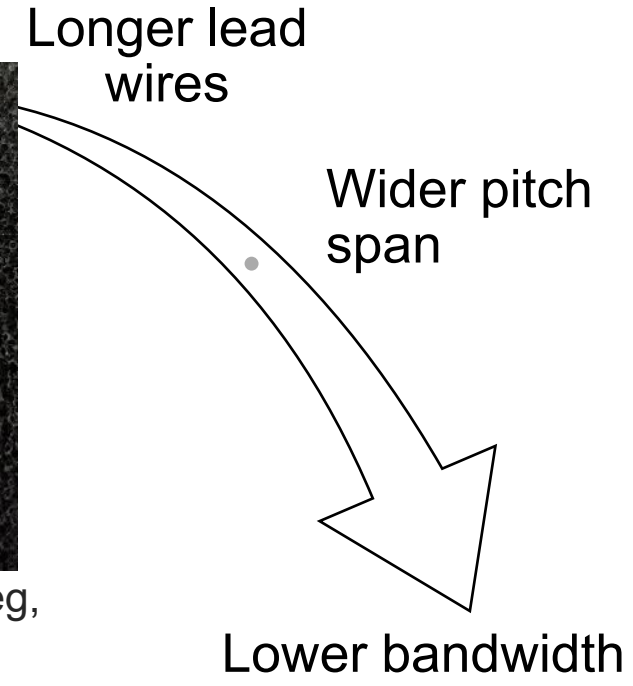
7mm, 60 deg, 4.4 GHz



11mm, 0 deg, 5 GHz



11mm, 60 deg, 3.3 GHz



Bandwidth is reduced with increased lead wire length and loop area created by two input leads. **Keep it short and a small loop area.**

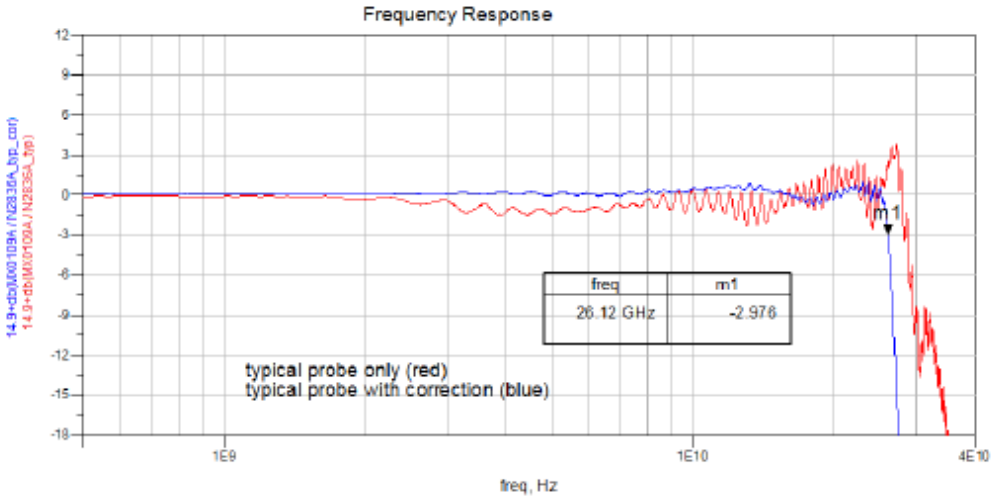
Enhanced Probe Response with DSP Correction

- To address the need for better performance and increased accuracy, **high performance probes started utilizing measured response of the probe system** to DSP correct and enhance the hardware response.

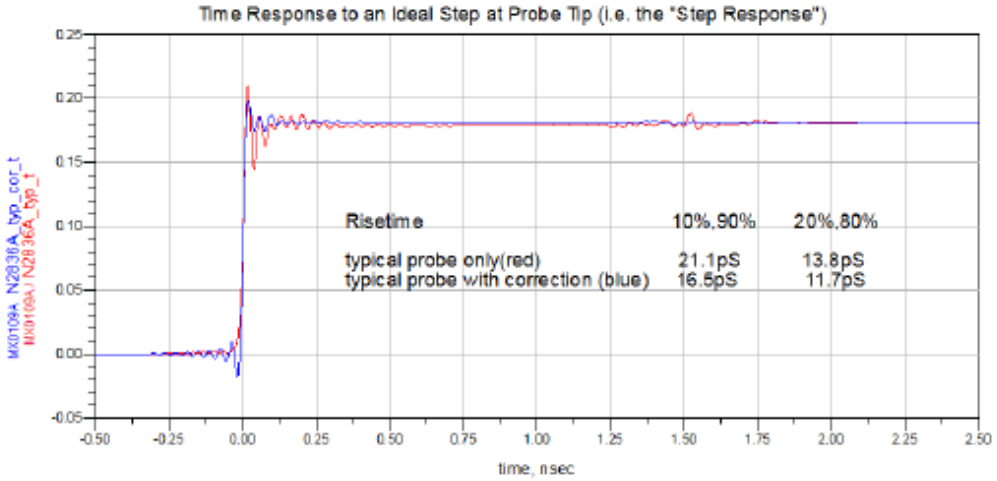
- Currently, **Keysight InfiniiMax II, III and III+ probe systems use S-parameters for correcting probe responses.** No correction for InfiniiMax I.

- On the probe menu of the Infiniium software, **you can choose the S parameter of a probe head** in the probe head selection menu. It is combined with the S parameter of the probe amp to correct the response of the whole probe system.



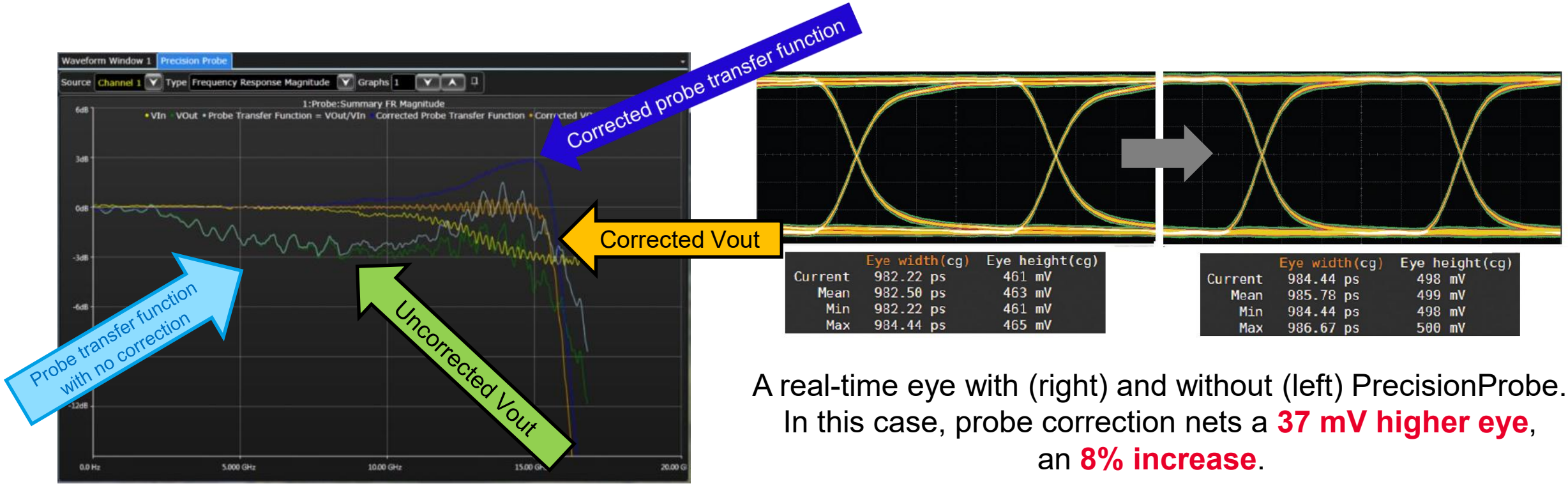


Red = before correction
Blue = after correction



PrecisionProbe – Advanced Response Correction Method

- The ideal way to ensure the best accuracy for a probe is to perform a calibration of its response ***in the configuration that it will be used*** before critical measurements are made.
- The PrecisionProbe application uses the fast calibration step signal and a high quality probe fixture with cables to accurately measure and correct for the response of any probe.



A real-time eye with (right) and without (left) PrecisionProbe. In this case, probe correction nets a **37 mV higher eye**, an **8% increase**.

Infiniium High-Performance Real-Time Oscilloscopes

Comparison of real-time oscilloscopes series by bandwidth







MXR-Series
Models from
500MHz to 6GHz

Available MSO models and HW serial trigger

V-Series
Models from
8GHz to 33GHz

UXR-Series
Models from 10GHz to 110GHz

Number of Channels

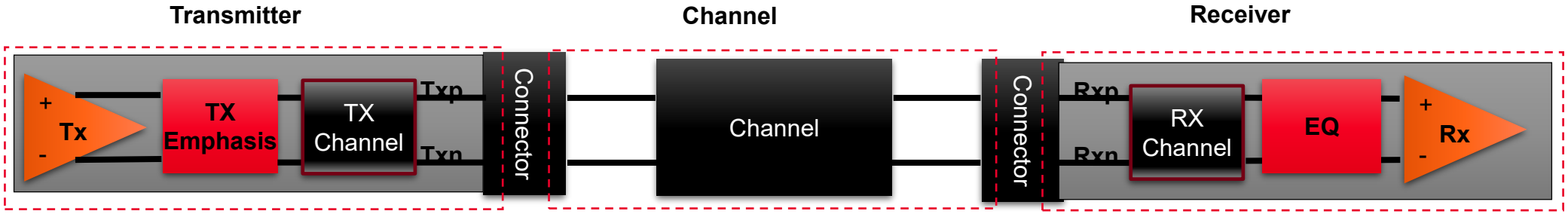
8
6
4
2

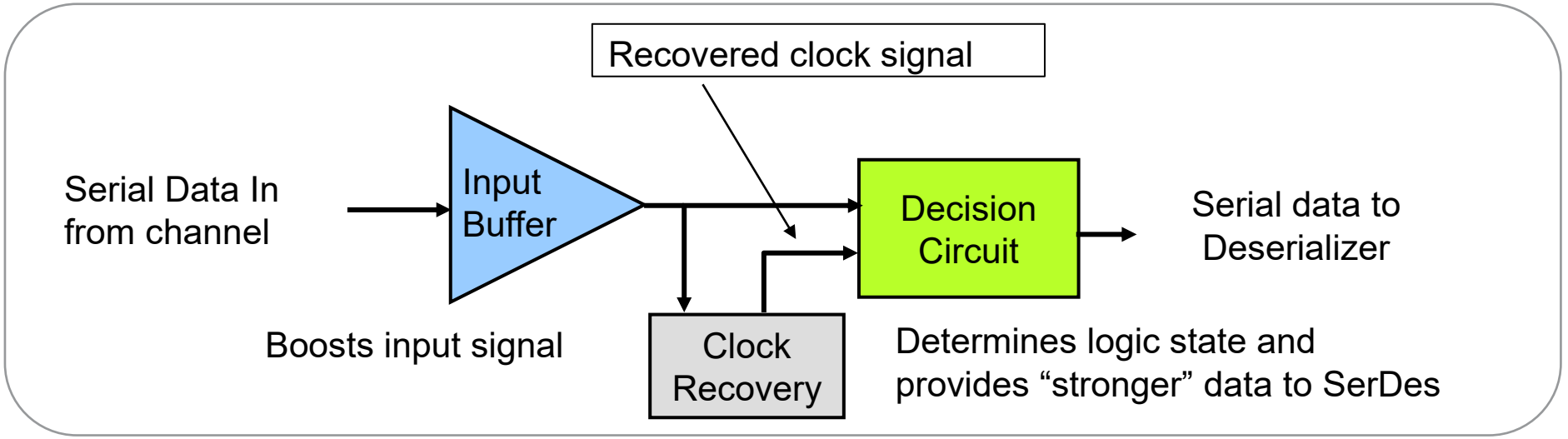
4 GHz 6 GHz 8 GHz 10 GHz 16 GHz 20 GHz 33 GHz 63 GHz 110 GHz

Unrestricted Maximum Bandwidth

Receiver Testing

What is inside of a receiver?

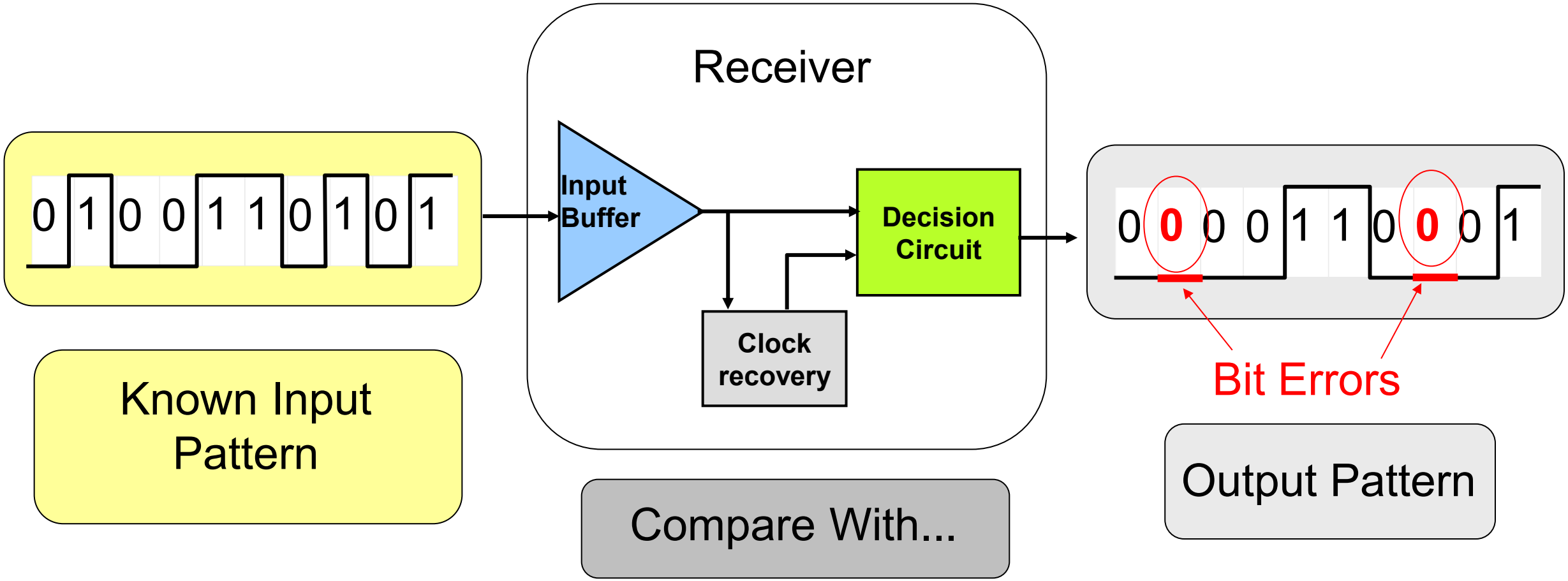




- Clock recovery creates timing reference from the incoming data stream
- Used to clock the decision circuit (also referred to as the “slicer”) to sample the data and determine logic state

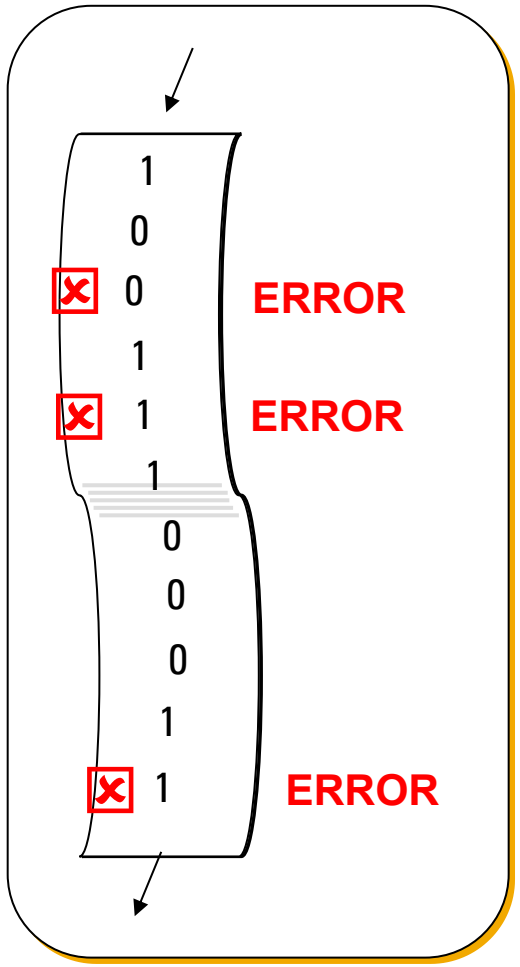
Receiver Testing

Testing the Receiver – BER instead of Eye Measurements



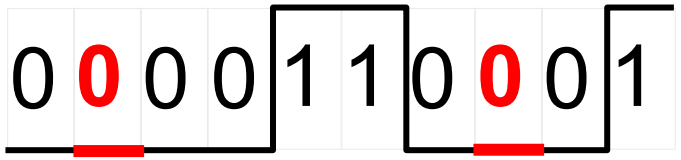
Receiver Testing

Testing the Receiver – What is BER?



"Bit Error Ratio"

I've sent 100 million bits….
How many were received OK,
How many were received in error?



$$\text{BER} = \frac{\text{Number of bits received in error}}{\text{Total number of bits received}}$$

e.g. BER = 1E-12 = 1 error every trillion bits (1,000,000,000,000)

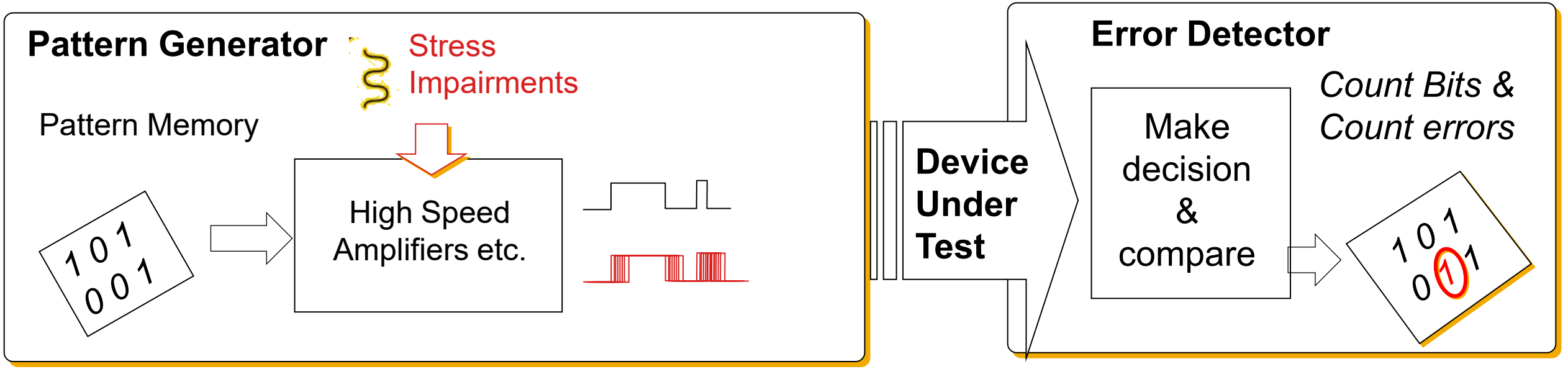
Receiver Testing

Introducing the BERT

- The Bit Error Ratio Tester is the basic instrument used for receiver testing
- The BERT is comprised of two main components:
  - **Pattern Generator – emulates transmitter & channel**
  - **Error Detector – counts bits and errors**



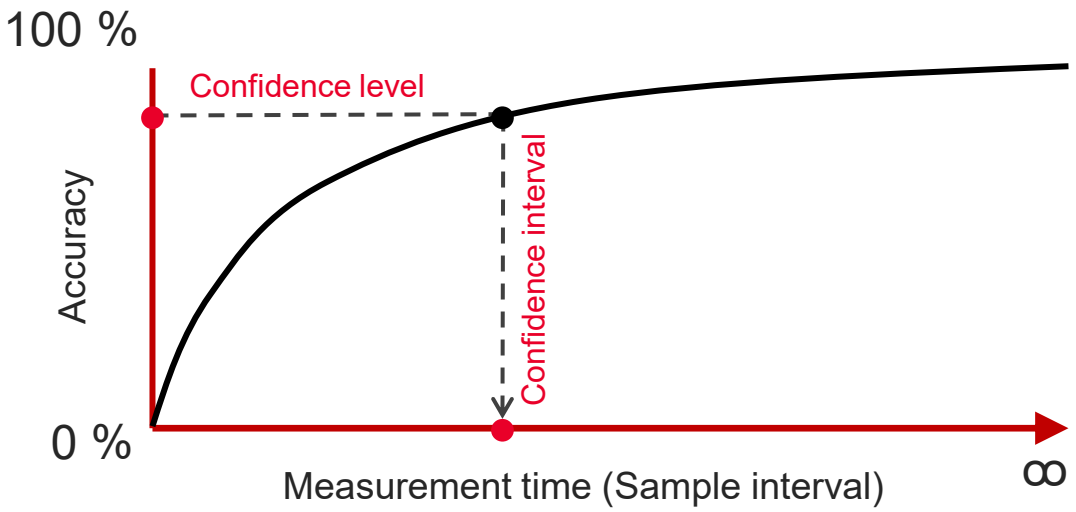
M8050A 120 GBd High Performance BERT



Receiver Testing

Measuring BER with a BERT

- In most links, errors occur randomly
- Any BER measurement is sampled for a *reasonable* amount of time
- 100.0000% accuracy can only be achieved with an infinitely long measurement sample



Accuracy increases with increased sample interval on an exponential asymptote.

- The 'Confidence Interval' determines how many bits must be sampled to achieve a given accuracy
- Many BERTs allow the user to enter the desired confidence interval, and set the sample interval automatically

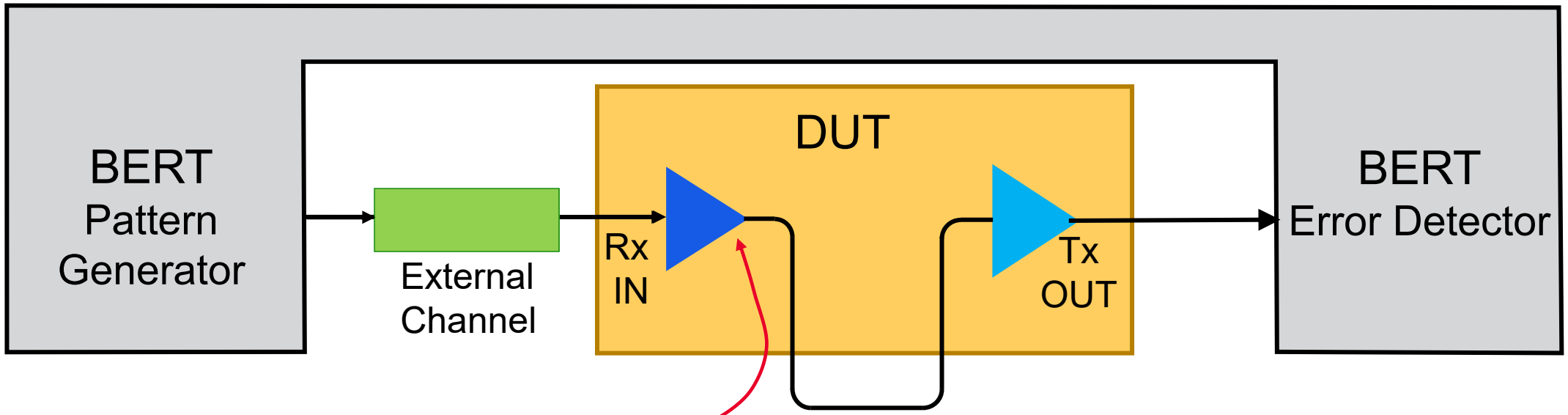
Receiver Testing

Test Patterns

- BERTs allow the user to select the test pattern
- Patterns can either be generated in hardware, or memory based
  - (More simple BERTs do not support memory based patterns)
- Hardware generated patterns include clock patterns (0101, 0011, 00001111, etc.) and PRBS
- **P**seudo **R**andom **B**inary **S**equence patterns emulate random data, but are defined by an algorithm
- Useful properties of PRBS patterns:
  - Easy to generate in hardware with a few exclusive OR gates
  - Pattern length is 2^n bits long, but generally shortened by 1 bit to have odd pattern length (what we generally state as 'PRBS-**n**' is actually 2^n-1 bits long)
  - Any PRBS pattern has the same number of 1s and 0s (offset by one for the shortened 2^n-1)
  - Any PRBS pattern can be divided by a power of 2, and results in the same PRBS pattern
  - A PRBS-n pattern will contain a string of n consecutive 1s followed by n-1 consecutive 0s

Receiver Testing

Basic test configuration using a BERT



Received data is here, inside the DUT

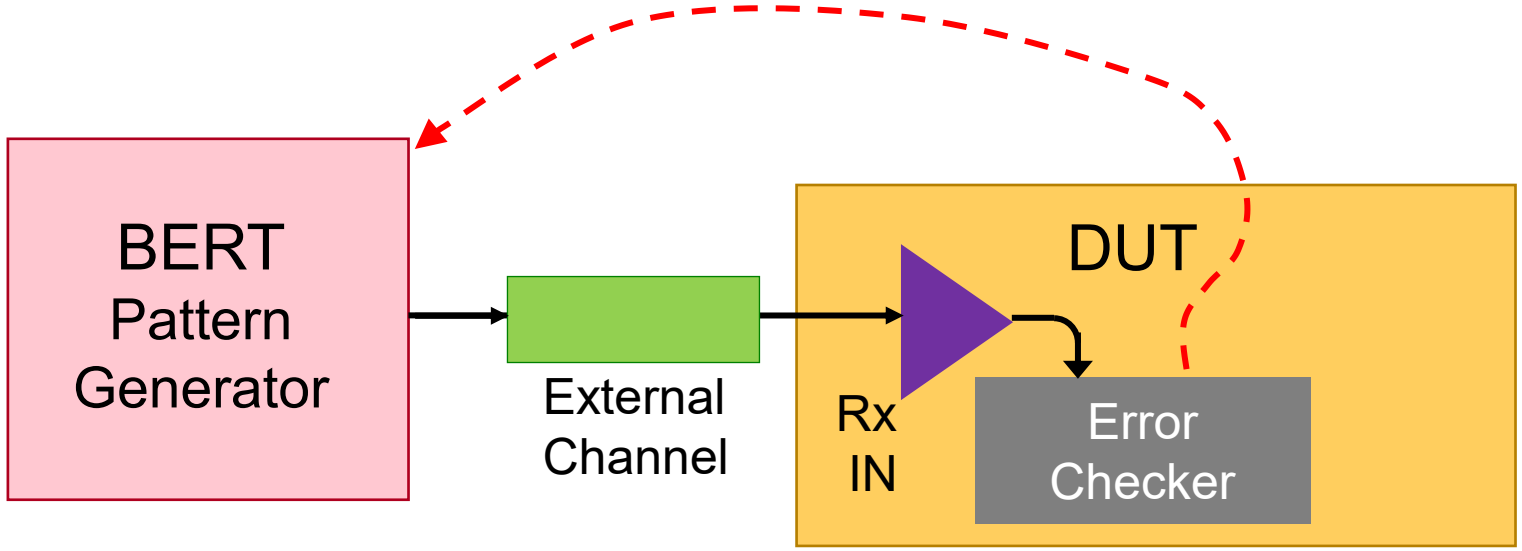
How do we get it into the error detector?

While the test data sent to the receiver input is impaired, the loopback path must be clean: Good DUT transmitter for loopback, short trace + cable to BERT error detector

Receiver Testing

DUTs with internal error checkers

- Some DUTs do not support loopback, but have an internal error counter instead
  - *May be necessary when the loopback link does not run error free (e.g. PAM4)*
- BERT PG is used for providing stressed pattern, but errors read directly from the DUT



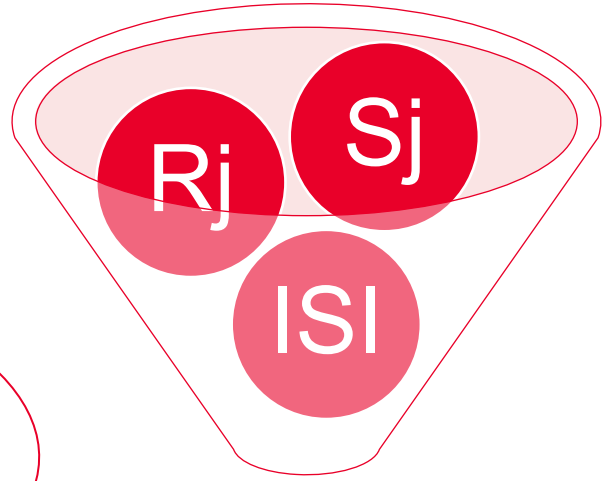
Stress Components in Pattern Generation

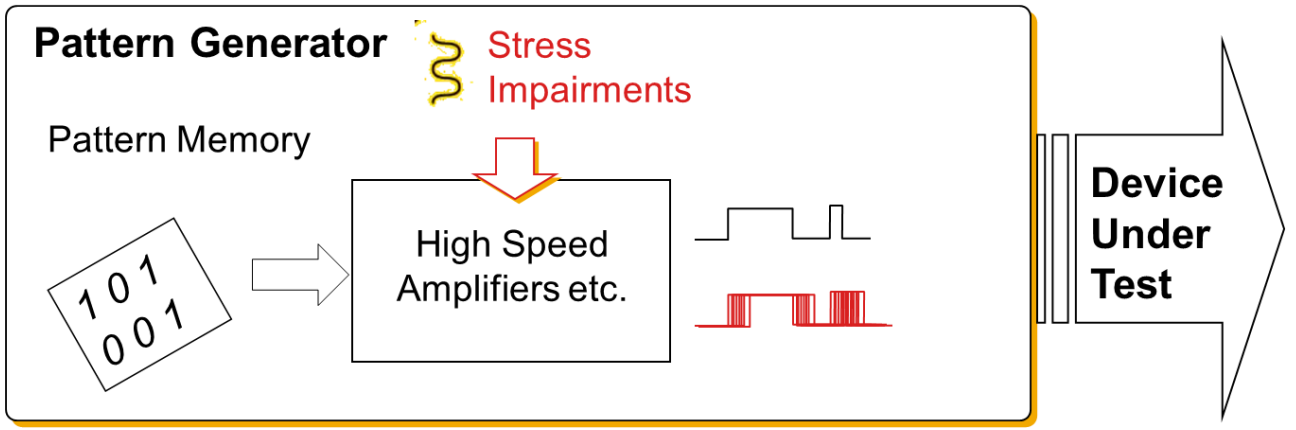
Three classes of stress signals may be used for an input/Rx test:

1. Jitter (Rj, Sj, etc.)
2. Interference
3. Crosstalk

Sets of stress components are also known as:

- ‘Jitter cocktail’
- ‘Stress cocktail’

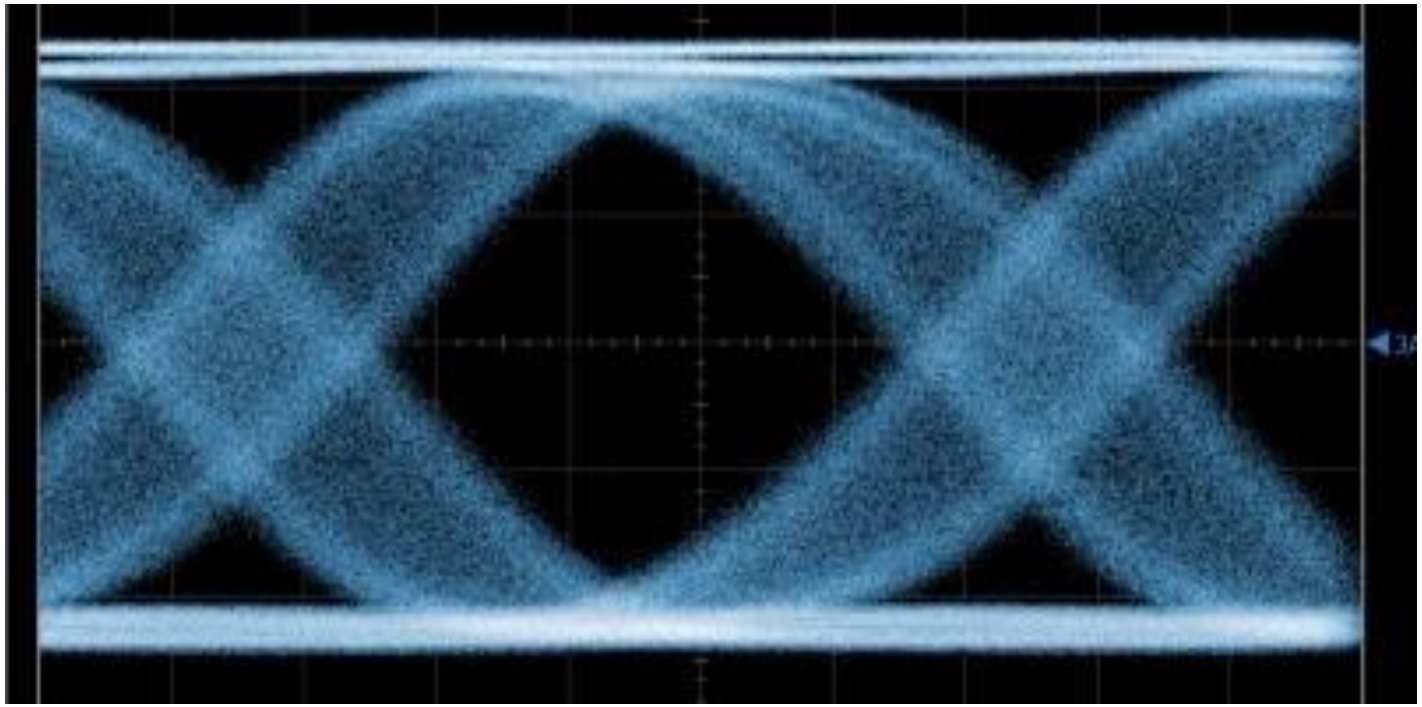






A Closer Look At Stress Components

1 **Jitter** – Horizontal eye closure



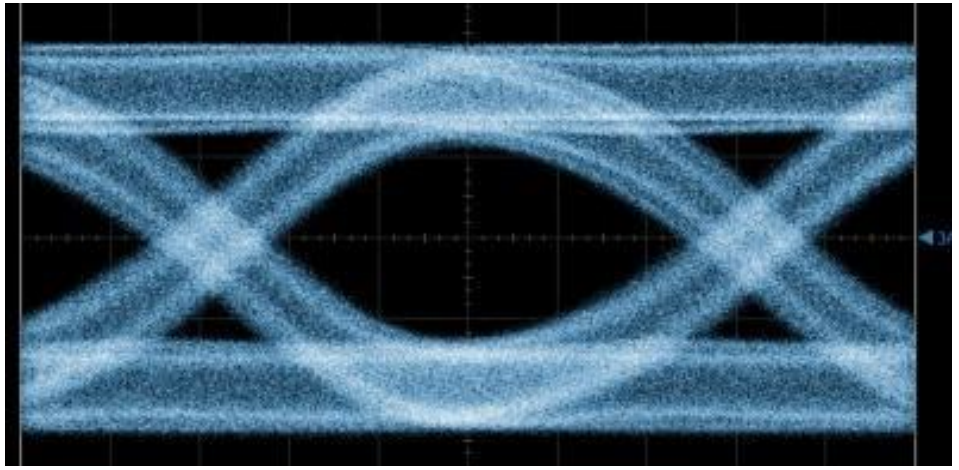
A Closer Look At Stress Components (continued)

2 **Interference** (Amplitude stress – vertical eye closure)

- Emulates noise coupled into channel
- Can be injected as differential mode (DMSI) or common mode (CMSI)
  - Differential mode tests detector and equalizer noise susceptibility
    - Standards may use random noise of sinusoidal noise
  - Common mode tests differential input CMRR – should not be in eye
    - CM tests generally use sinusoidal waveform



Internal or external interference sources can be used



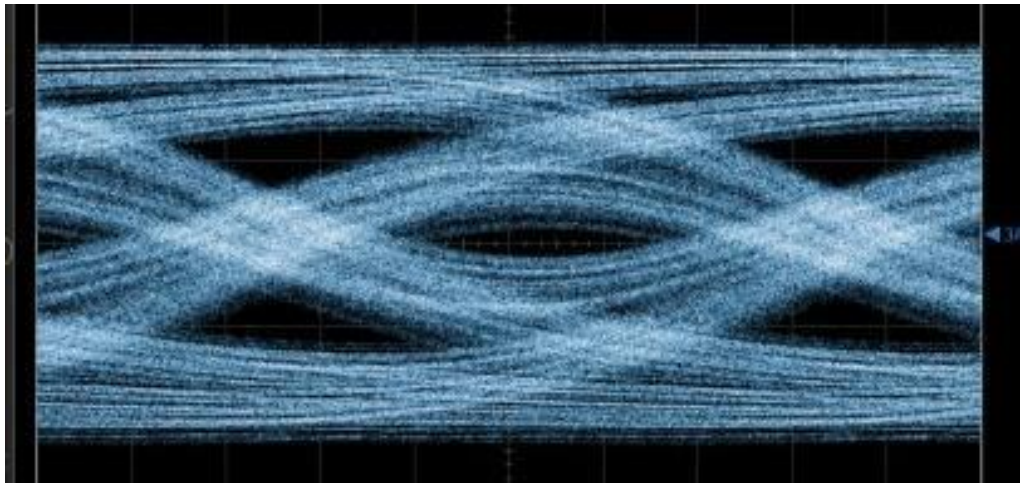
A Closer Look At Stress Components (continued)

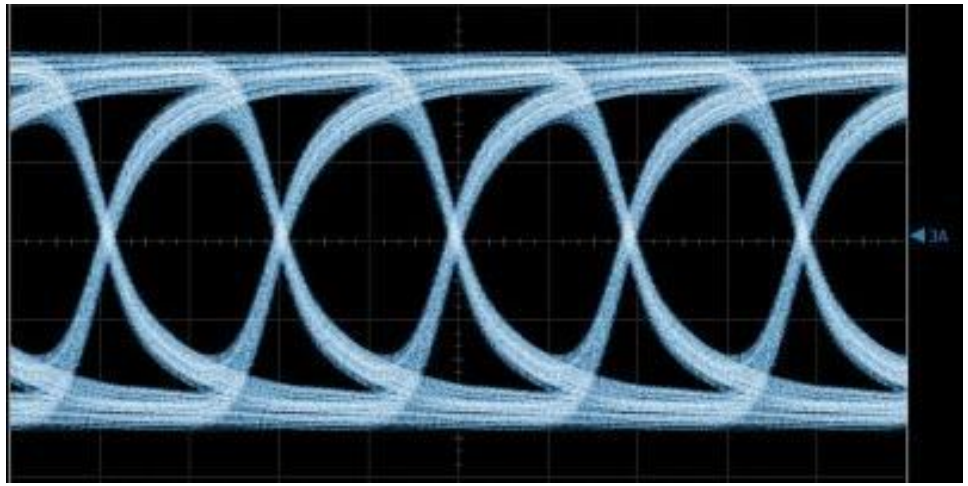


Hardware ISI traces can be used!

Inter Symbol Interference (ISI)

- Emulates frequency dependent channel loss through circuit board traces
  - Tests receiver equalization
  - Typically generated in real circuit board trace (a.k.a. Frequency Dependent Attenuator), outside of Pattern Generator
  - At higher data rates, interconnecting cables in test setup contribute significant portion of total ISI

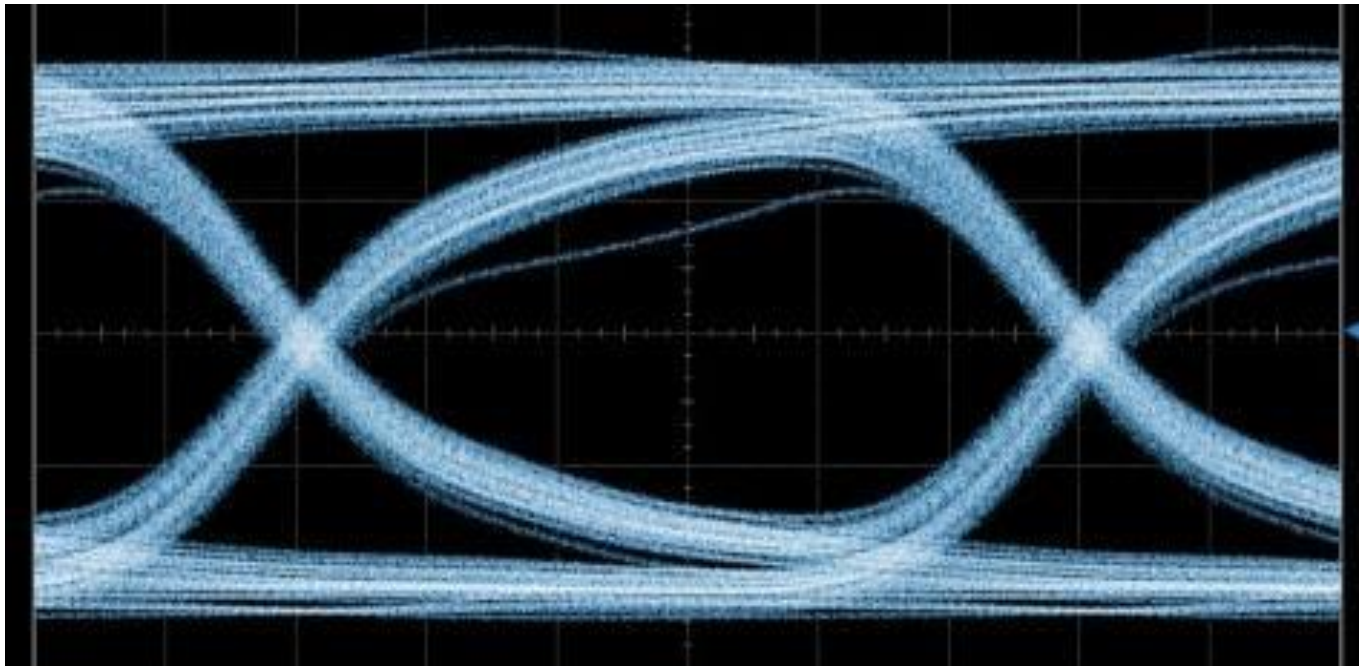




A Closer Look At Stress Components (continued)

3 **Aggressors** – Crosstalk emulation

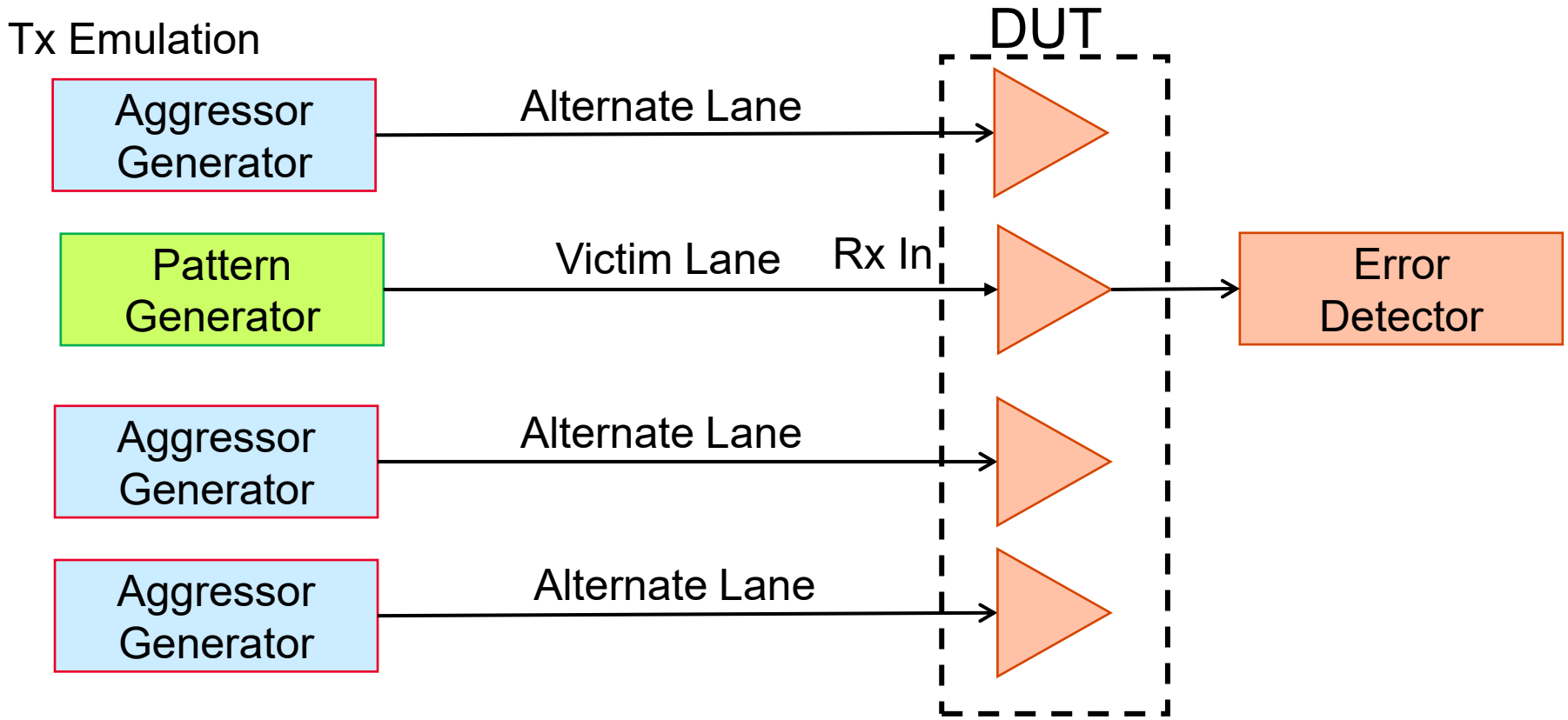
- Back channel in same lane – far end
- Alternate lanes – near end



A Closer Look At Stress Components (continued)

Crosstalk Aggressors

- Real aggressors in back channel and alternate lanes are better test than adding BUJ directly to victim lane



Find the BERT Solution That's Right for You

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M8020A J-BERT
32 Gb/s NRZ



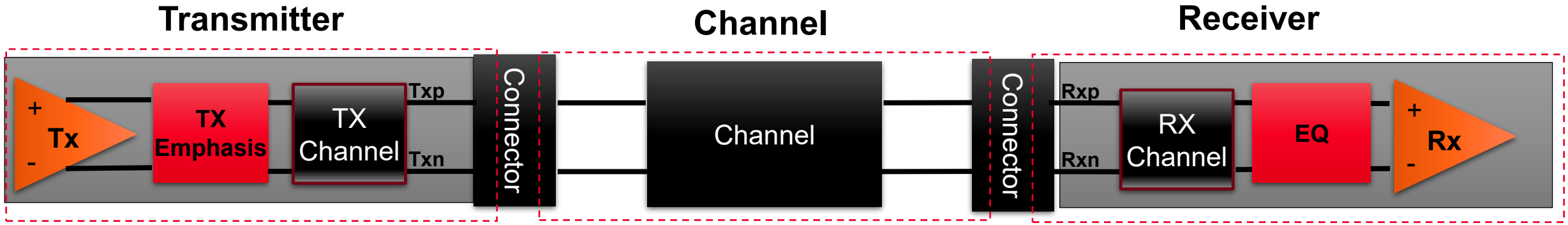
M8040A BERT
64 GBd NRZ & PAM3/4



M8050A BERT
120 GBd NRZ & PAM4/6/8

Whether you are working on data center or computing technologies, Keysight BERTs enable physical layer characterization, verification, and compliance testing of your receiver for both NRZ and PAM4 coding schemes. Master your next design with flexible modules, intuitive software, advanced analysis applications, and expert-level support.

Conclusion and Highlights





Real-time Oscilloscope (UXR)



Equivalent-time Oscilloscope (DCA)



Network Analyzer (PNA, ENA)



TDR/TDT (DCA)



Bit Error Ratio Testers (BERT), Pattern Generators (PG), Arbitrary Waveform Generators (AWG)

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