


# Dynamic Behavior of Voltage Sources

## A Short Introduction to Power Integrity

x.test Praxisseminar, Graz

2026-09-09

OMICRON LAB

# Agenda

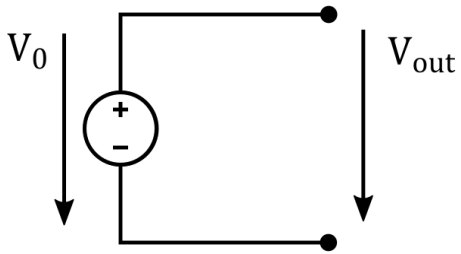
- DC voltage source (ideal vs. real)
- Control loop stability
- Output Impedance of VRM
- From the power to the load
- Measuring PDN Impedance
- Examples & Hands-On



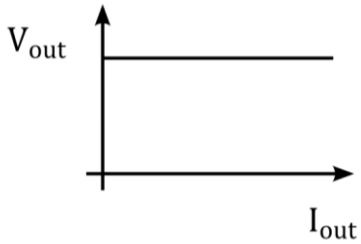
# Back to Basics: DC-Voltage Source

Two-terminal device that maintains a constant DC-voltage.

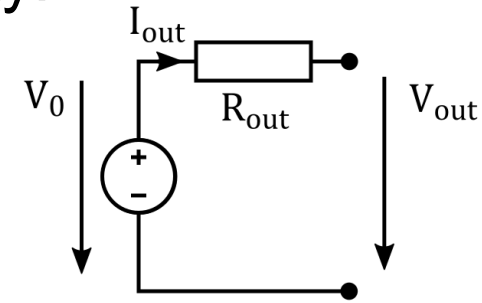
Ideally:



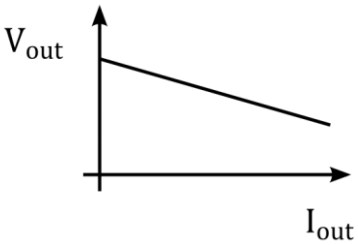

$$R_{out} = 0 \rightarrow V_{out} = V_0$$



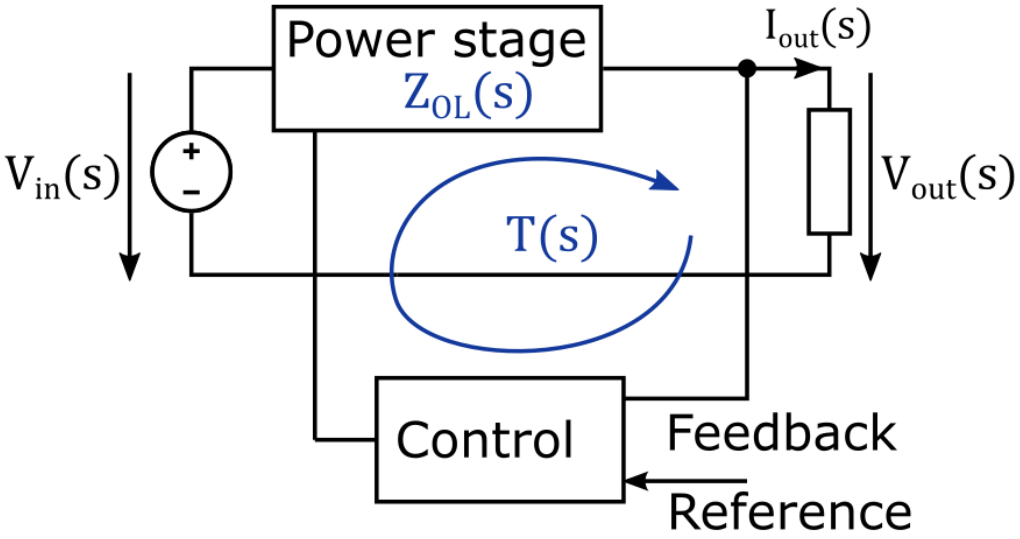

In reality:




$$R_{out} \neq 0 \rightarrow V_{out} = V_0 - I_{out}R_{out}$$



# Stabilizing Output via Voltage Feedback



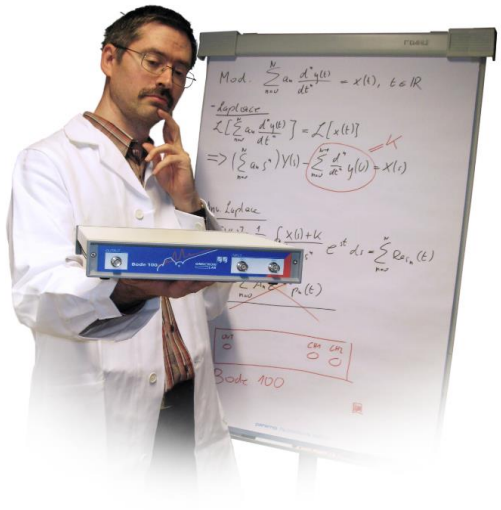

- Closing the loop changes the output impedance to:

$$Z_{out}(s) = \frac{Z_{OL}(s)}{1 + T(s)}$$

$T(s)$...Loop Gain
$Z_{OL}(s)$...Open-Loop Output Impedance
$Z_{out}(s)$...Closed-Loop Output Impedance

# Closed-Loop Output Impedance

$$Z_{out}(s) = \frac{Z_{OL}(s)}{1 + T(s)}$$



- If $T(s) \gg 1$ then $Z_{out}(s) \ll Z_{OL}(s)$
- If $T(s) \ll 1$ then $Z_{out}(s) = Z_{OL}(s)$
- If $T(s) = 1$ then $Z_{out}(s) = ½\ Z_{OL}(s)$

➢ High loop gain results in low output impedance

# Loop Gain

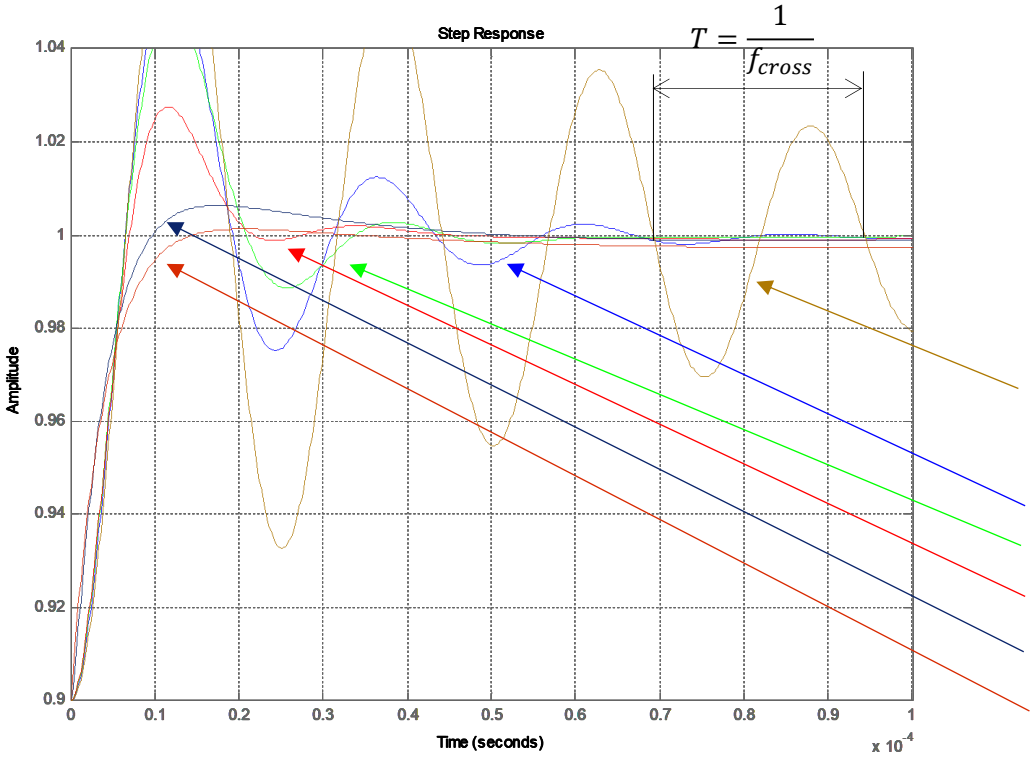
- Loop Gain at DC is not $\infty$ → $R_{out} \neq 0$
- Control loop is not infinitely fast → Loop Gain reduces with $f$
- Loop Gain crosses $0\ dB$ line at some crossover frequency $f_c$
- $f_c$ Is the natural frequency of the closed-loop system

➢ Control loop affects $Z_{out}$ mainly below $f_c$

➢ Above $f_c$ the feedback has nearly no effect: $Z_{out}(s) = Z_{OL}(s)$

# Phase Margin improves Stability

Example: Voltage-mode Buck Converter Reference to Output Step




Simulation of synchronous Buck Converter (CCM, small signal)
15 V to 1 V step down
300 kHz switching frequency
≈40 kHz crossover frequency

$\varphi_m = 7.4° \rightarrow$ High overshoot + ringing

$\varphi_m = 23°$

$\varphi_m = 31°$

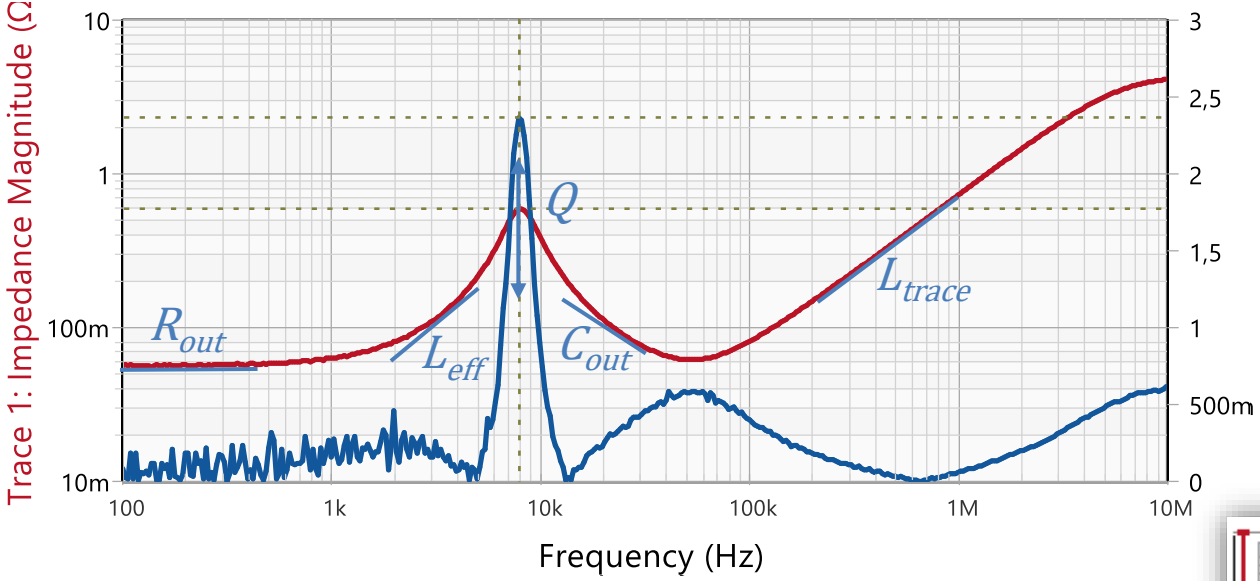
$\varphi_m = 45°$

$\varphi_m = 78° \rightarrow$ Highly damped

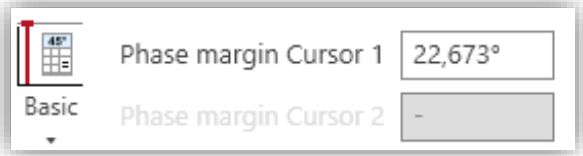
$\varphi_m = 87°$

# NISM (Non-Invasive Stability Measurement)

- Q correlates to Phase Margin $\varphi_m$
- Peak in $Z_{out}$ correlates to the Q of the closed loop system

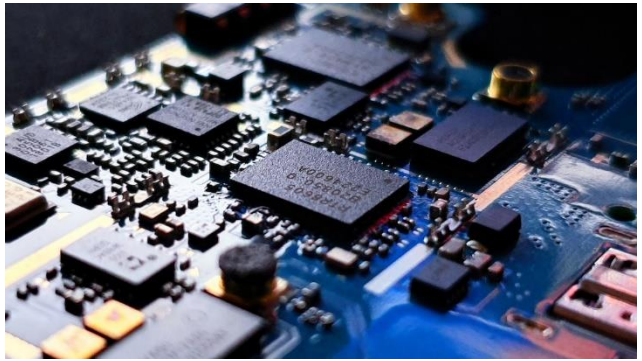



$$Q = \frac{\sqrt{\cos(\varphi_m)}}{\sin(\varphi_m)}$$

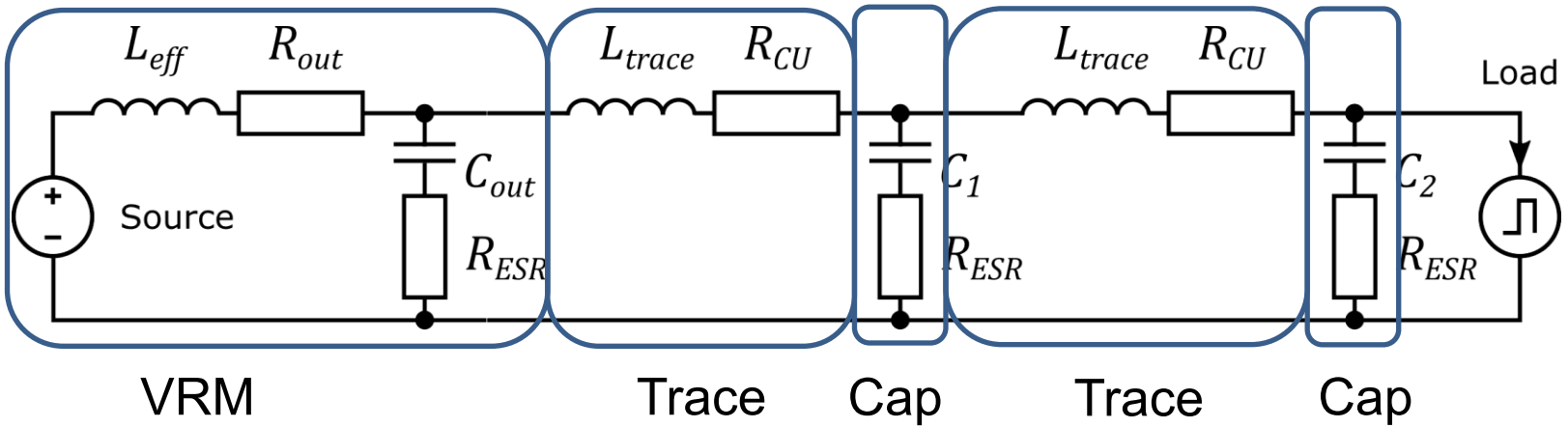


# Power Distribution Network (PDN)

- Power source and input filters
- Voltage Regulator Module (VRM)
- Point of load regulator (POL)
- Output filtering (ferrites, capacitors)
- PCB lines, board planes, vias, capacitors
- Package leads, planes, bond-wire, on-die capacitance
- Return path (ground plane)

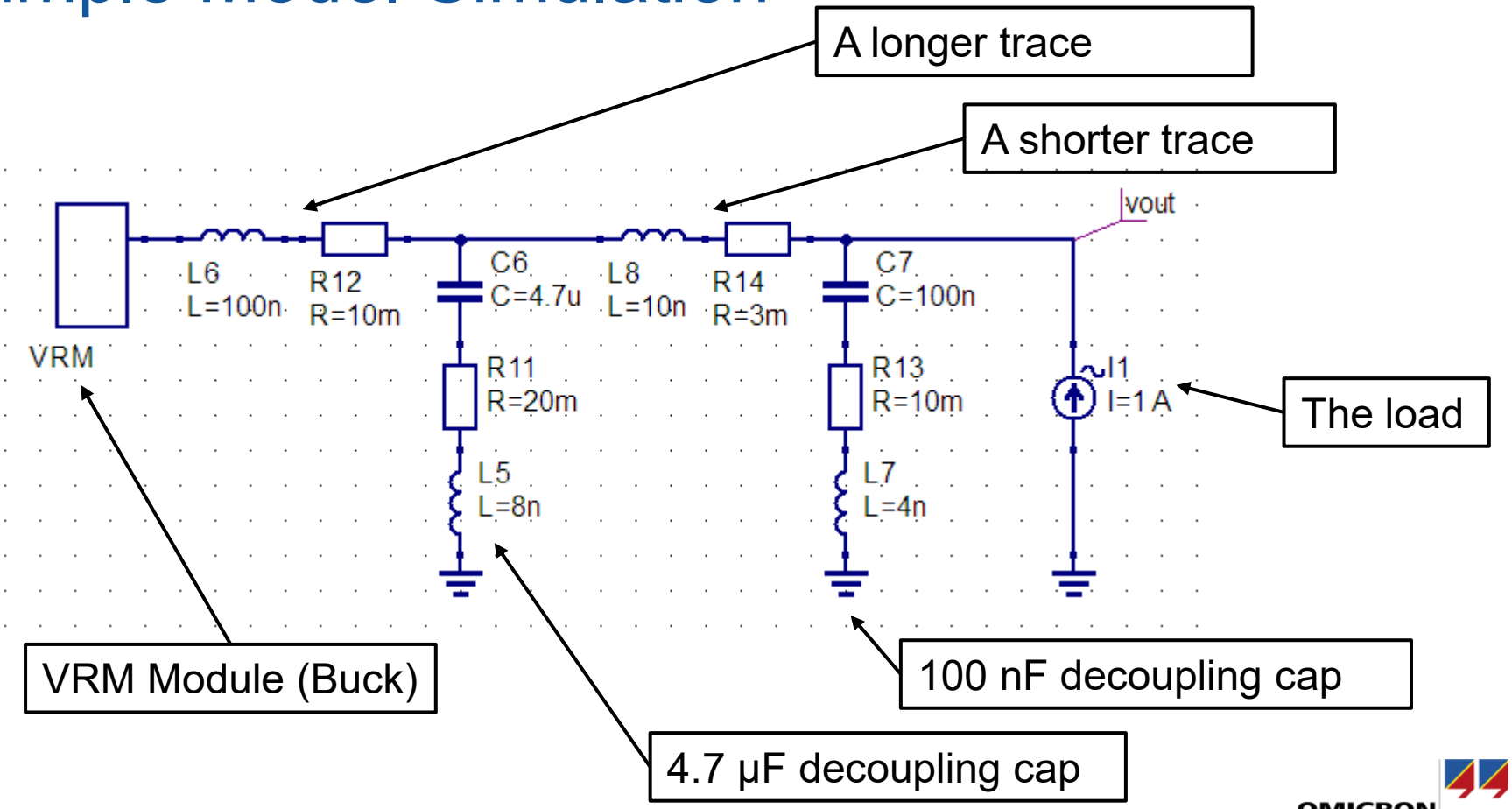


# A Simple PDN Model

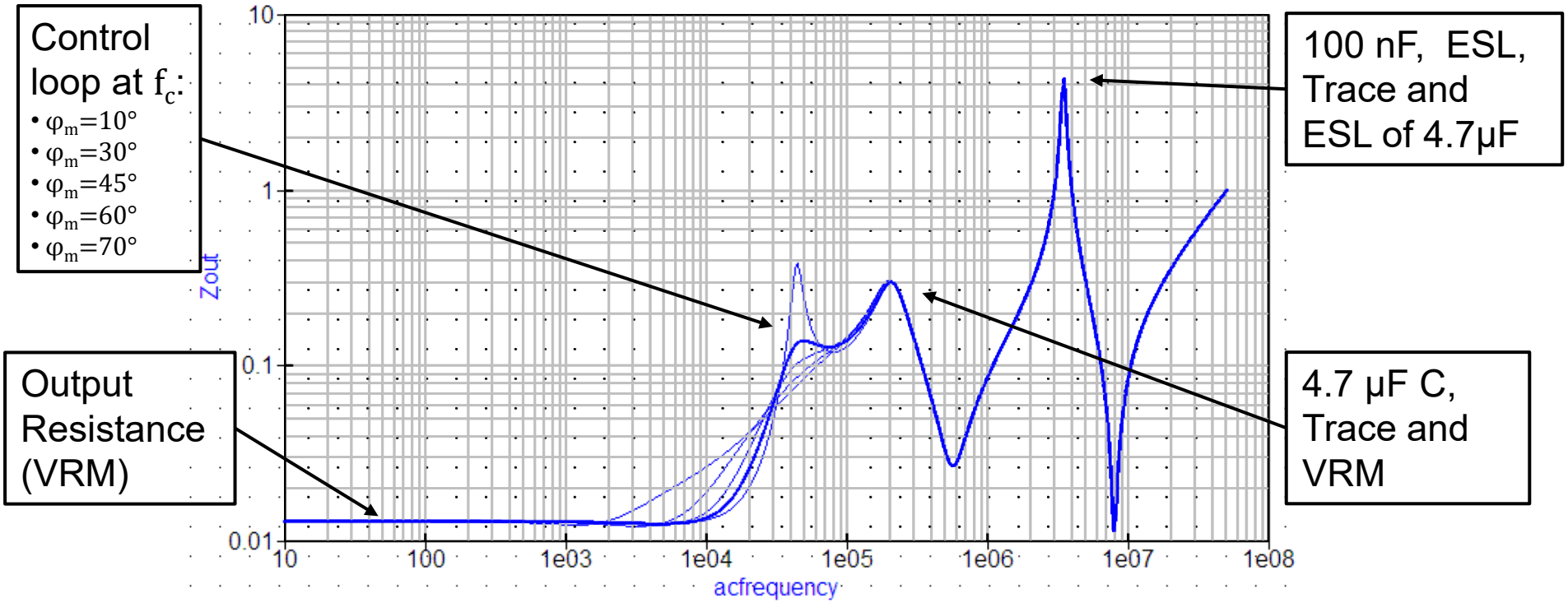



- Multiple L-C resonance circuits
  - Ceramic caps have generally very low ESR values.
  - Ferrites have generally low resistance.
  - The Q of the resonances can be high.

# Simple Model Simulation



# Impedance Profile at the Point of Load



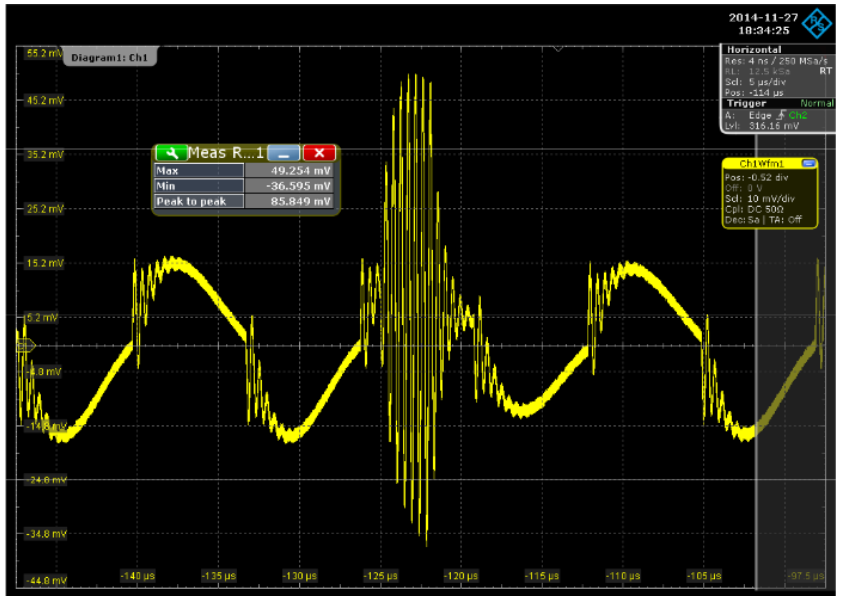

- 200 kHz load current → 300 mΩ source impedance.
- 3 MHz load current → 3 Ω source impedance.
- ➢ 1 A load current causes 0.3V / 3 V drop.

# Avoid Supply Impedance Peaks

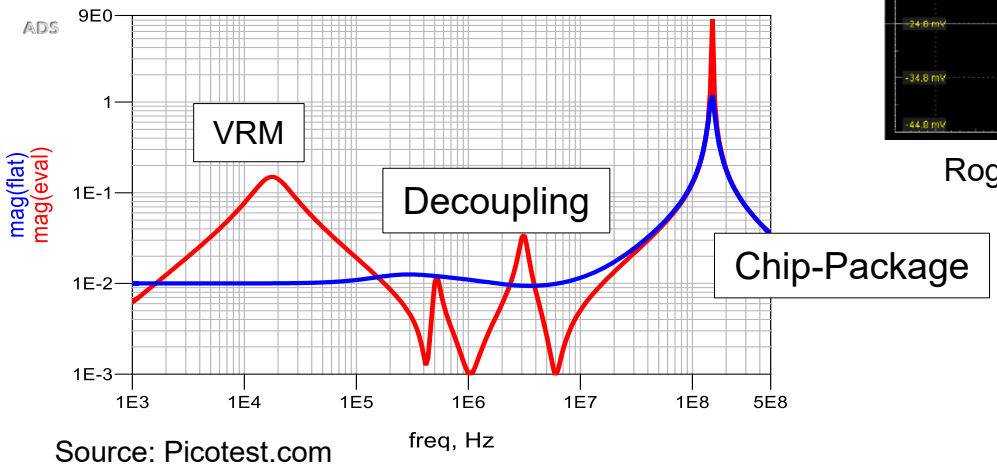
- Can violate the target impedance
- High impedance increases the risk of coupling noise to the supply voltage ($V = \sqrt{P \cdot R}$)
- Noise on the supply voltage can degrade performance of oscillators (Jitter), reference voltages, ADCs, low-noise amplifiers etc...
- And in worst case, they can stack...

# Risk of Rogue Waves

- Dynamic load currents at multiple frequencies can superimpose.
- Worst case scenario is a “Rogue wave”.
- “Flat Impedance Approach” can safely avoid this risk.




Rogue Wave captured by Steve Sandler (Picotest)

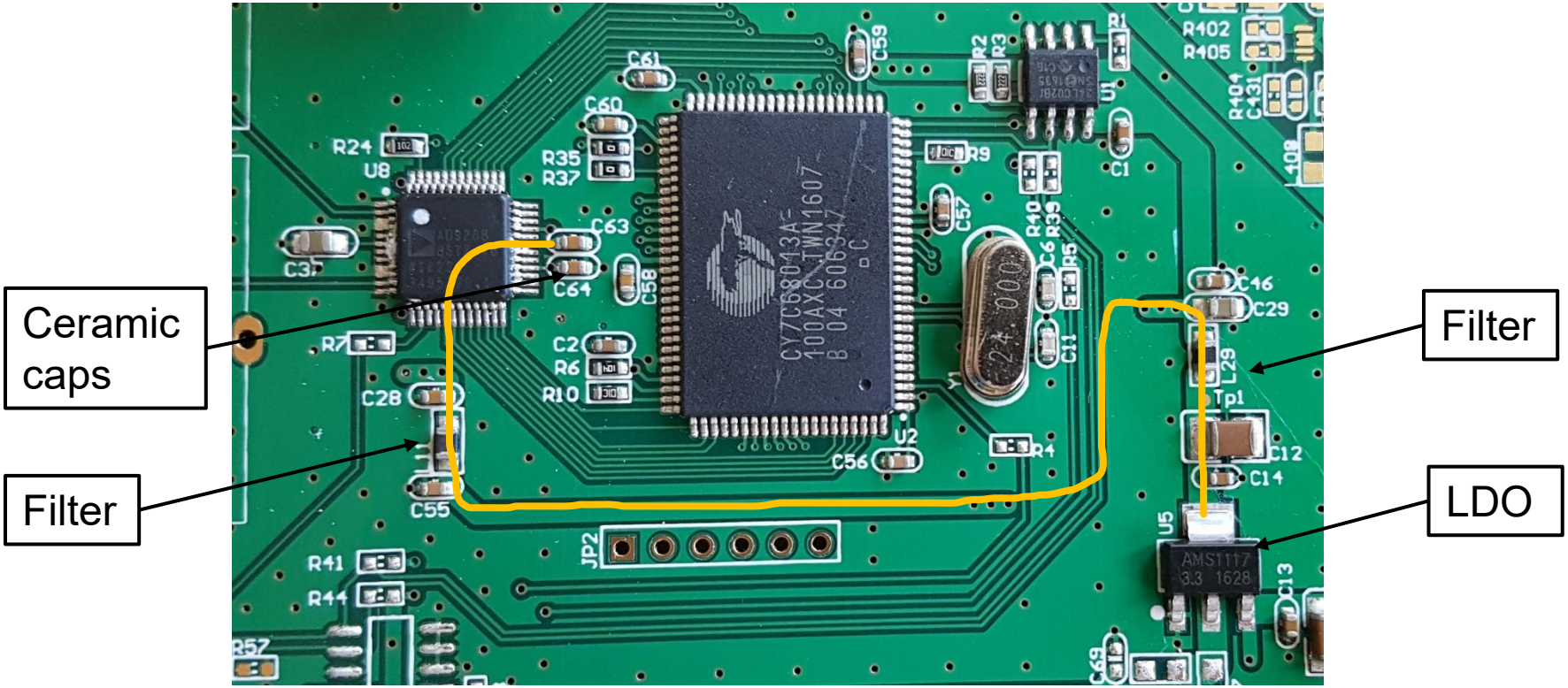



Source: Picotest.com

# System-Example: USB Scope

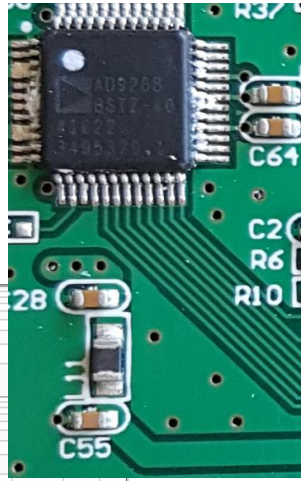


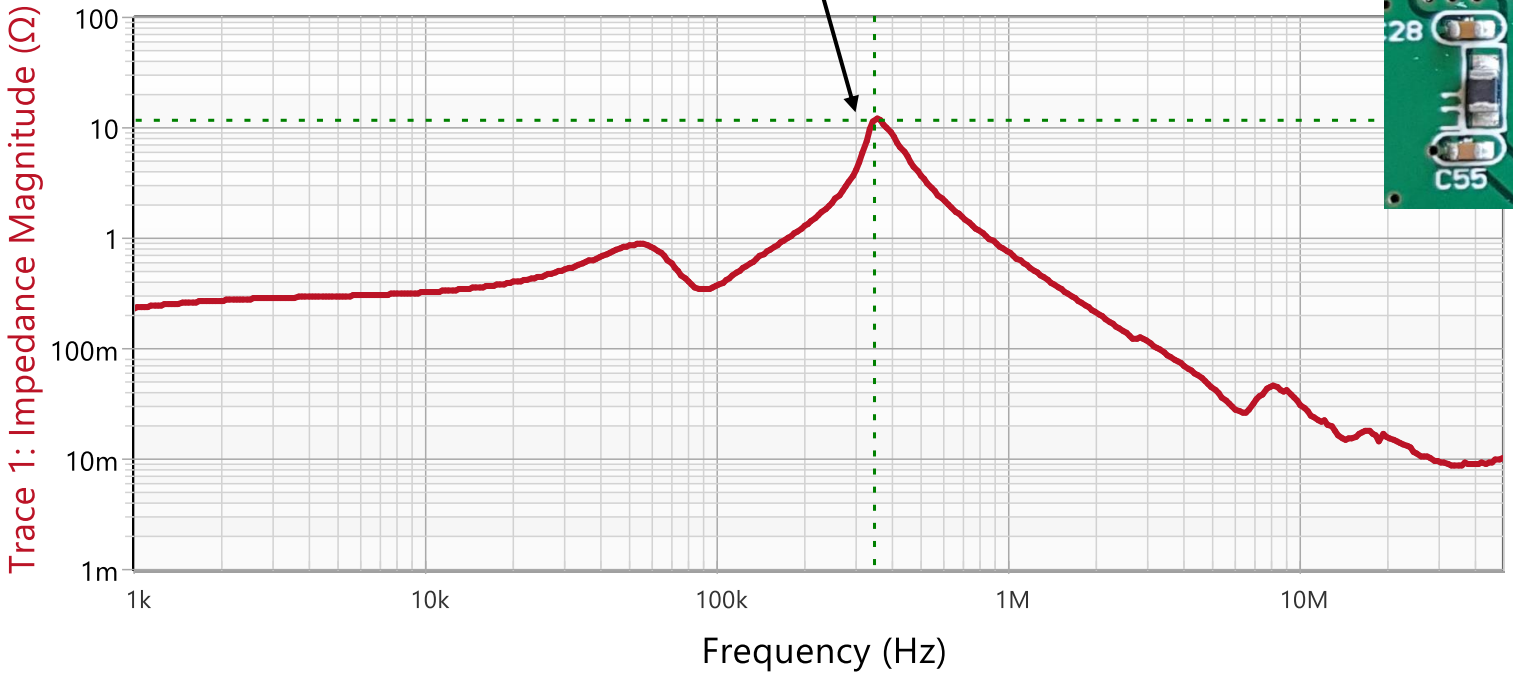
# ADC Power Supply



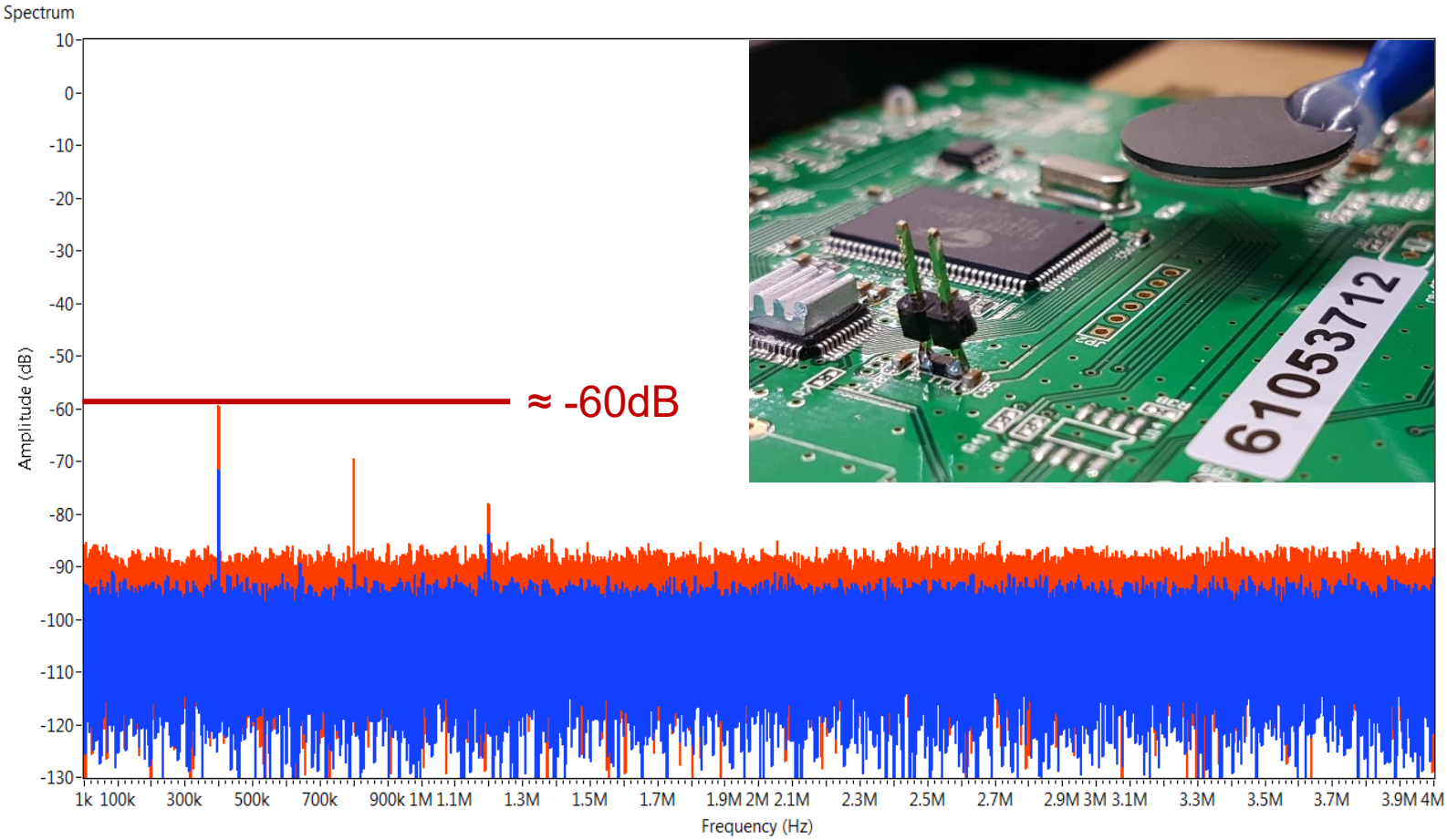
# Impedance Profile at ADC

High resonance peak at 300...400 kHz
Caused by SMC ferrite and ceramic caps.

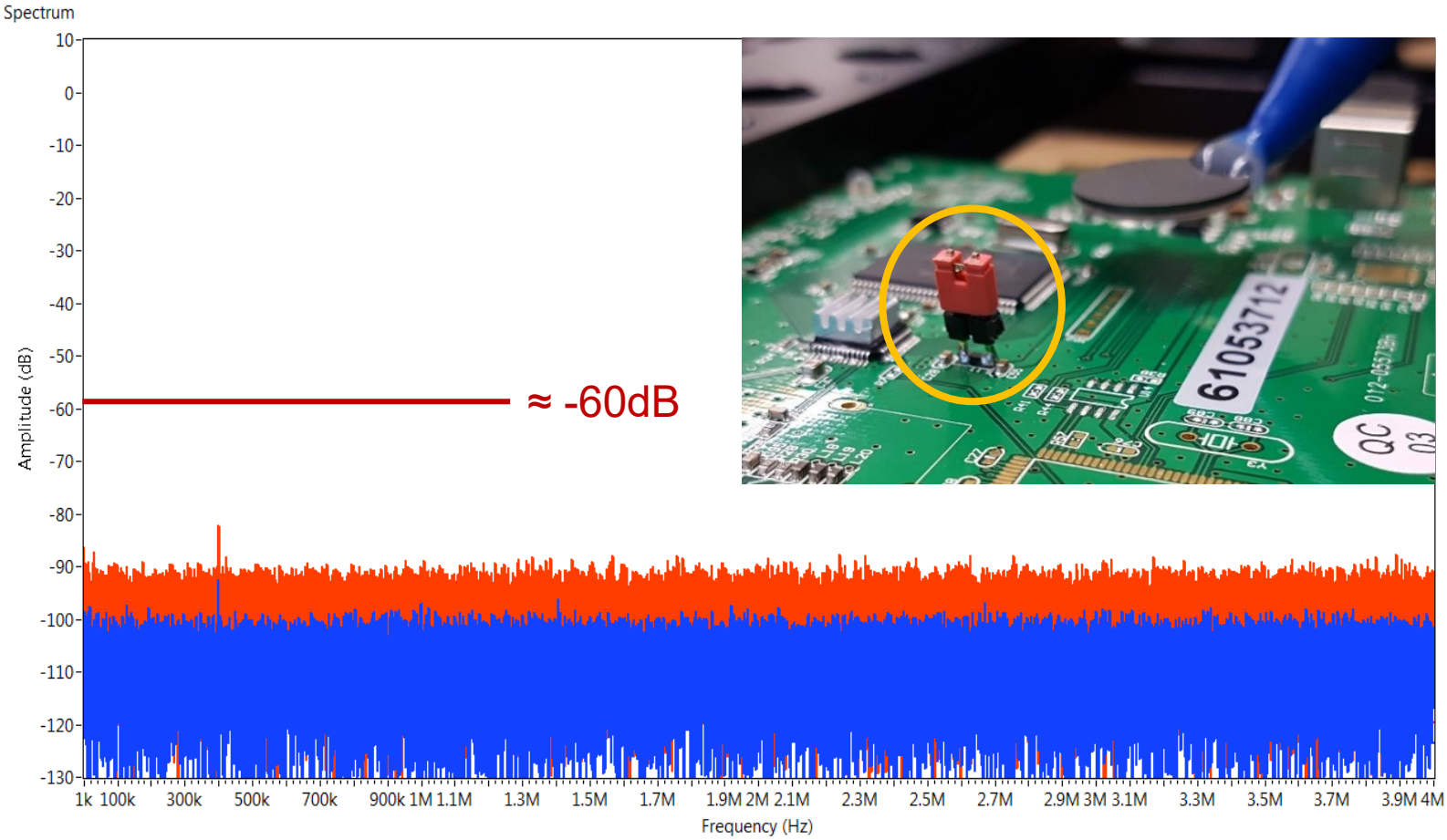


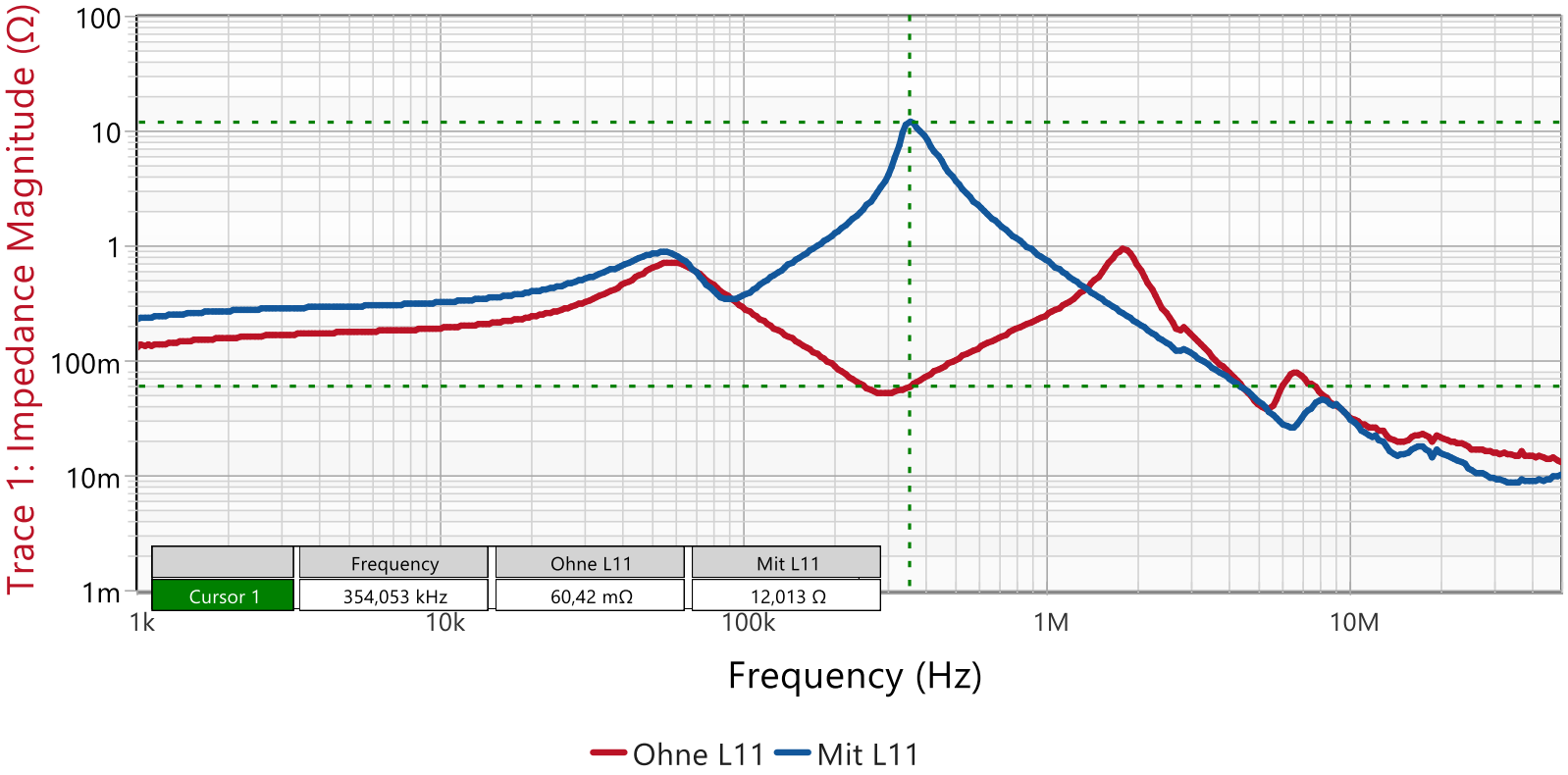
# 400 kHz Disturbance (inductively coupled)



# Shorting the Ferrite Bead



# What has Changed in Output Impedance?

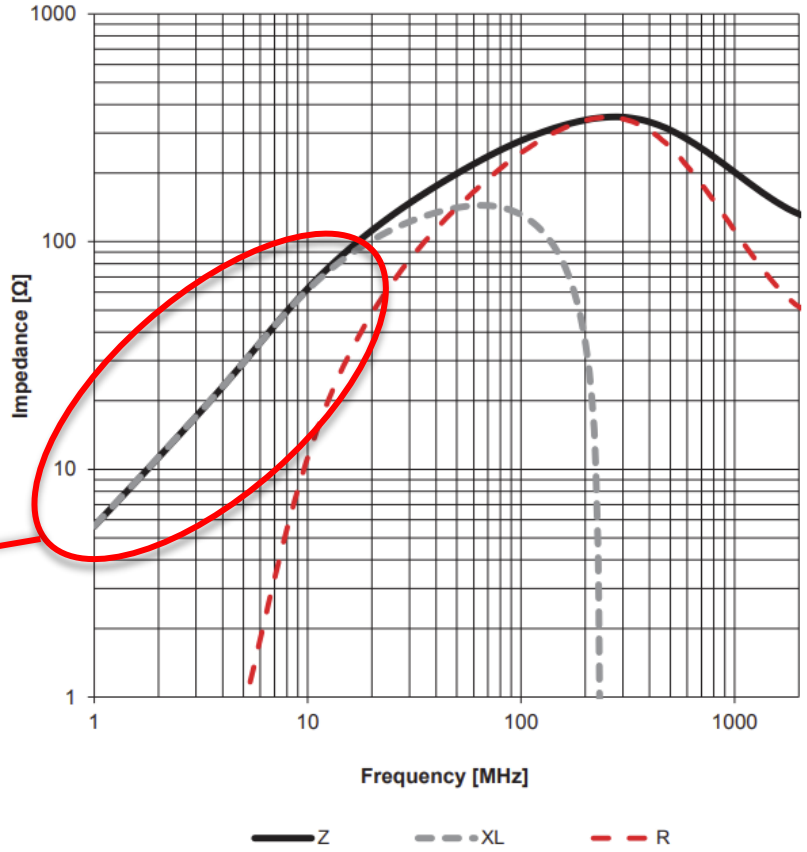


# The Risk of Ferrite Beads

- At high frequency (10s of MHz) lossy and “resistive”
- At dc they represent a “small resistance” (e.g. 10mΩ)
- What happens at several MHz?

→Low loss inductor

→High-Q LC-parallel resonance!




https://www.we-online.com/components/products/datasheet/74279224271.pdf

# The PDN Impedance Plot

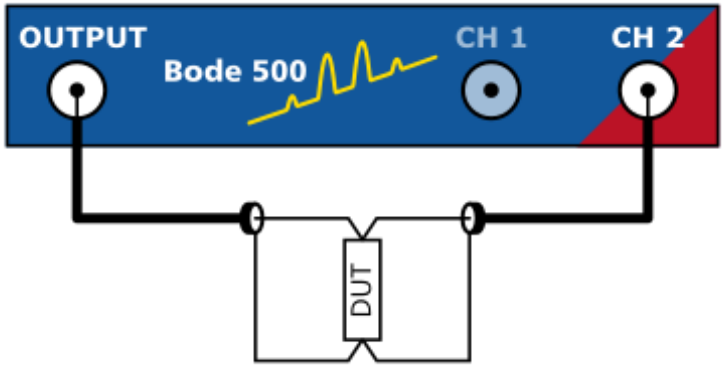
1. Can be a design goal in PDN design (target impedance).
2. Contains information about the stability (oscillation tendency) of the voltage regulator.
3. Reveals resonance frequencies of the decoupling network.



- Let's measure it!
- Challenge: **Very low impedance**

# 2-Port Shunt-Thru Measurement

- Provides high sensitivity for low impedance.
- Emulates a 4-wire kelvin connection.
- Can be used to measure into the µΩ range.
- Measures S21 and calculates Z via $Z = 25\Omega \frac{S_{21}}{1 - S_{21}}$



# Connecting Analyzer and DUT

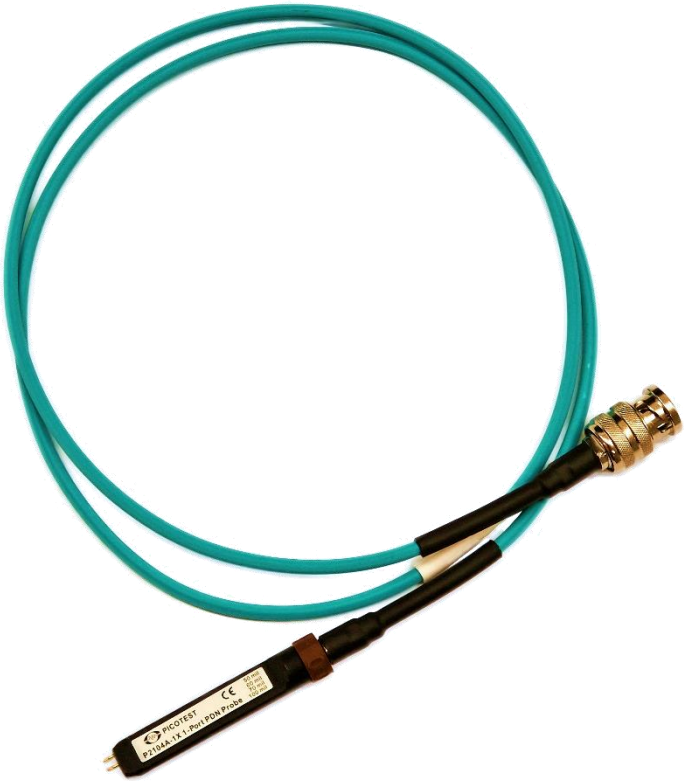



PCB with 0402, 0603, 0805, 1206 etc. SMD Pads

VNA with Type-N coaxial connectors

# Picotest PDN Probes

## P2104A One-Port Probe

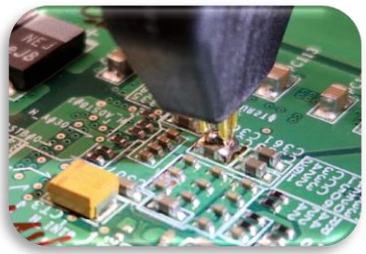
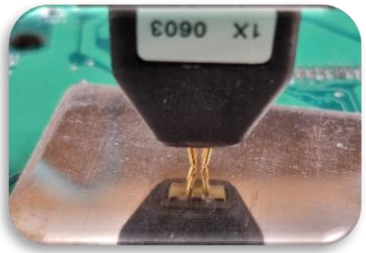



## P2102A Two-Port Probe



# Picotest PDN Probes

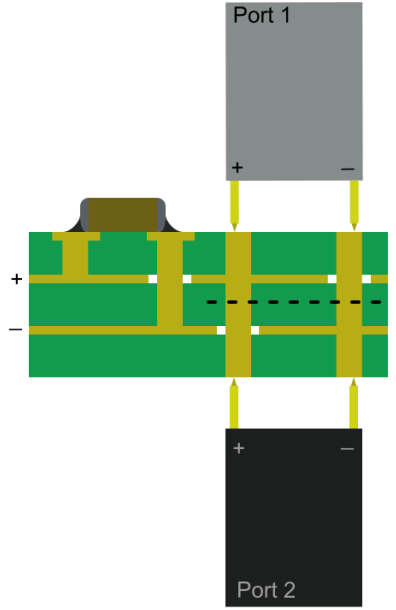
- High bandwidth & flat frequency response.
- Different coaxial connector styles (SMA, BNC, N).
- Picotest PDN Cable® (ultra high shield attenuation and ultra low shield resistance, highly flexible and thin).
- P2102A - four probe heads (0402, 0603, 0805, 1206).
- P2104A - different pitch sizes available (50mil-100mil).
- 1x, 2x, 5x or 10x attenuation options available.

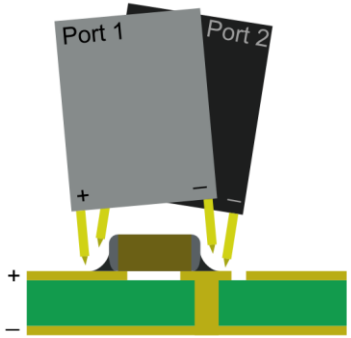





# 1-Port Probe vs. 2-Port Probe

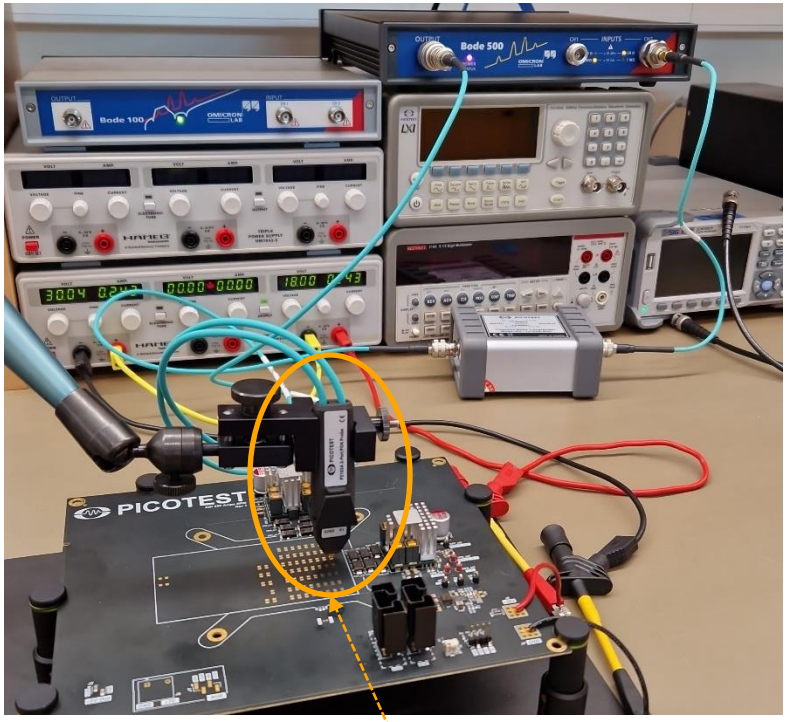
1. One-Port Probe (2 probes needed 😟)
   - 🙂 Flexible positioning
   - 🙂 Get into power planes by opposite placement
   - 🥵 Difficult handling (probe holder)
   - 🧐 Allows measuring transfer impedance
2. Two-Port Probe (only **one** 😀)
   - 🙂 Can by used “by hand” (browser probe)
   - 🙂 Very easy & intuitive to handle
   - 😟 Less flexible, no opposite placement



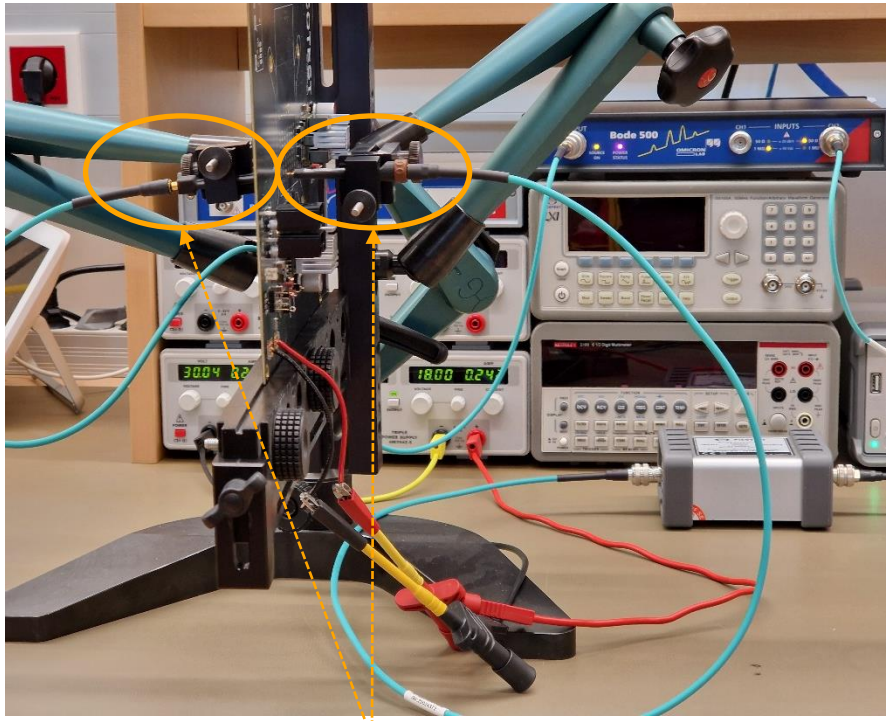



# Measurement Setup Example

Probe & PCB clamping: http://www.clampman.info/

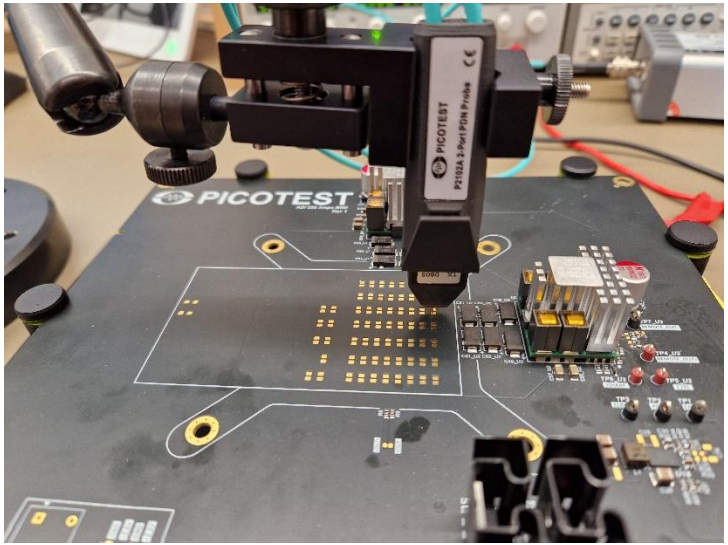


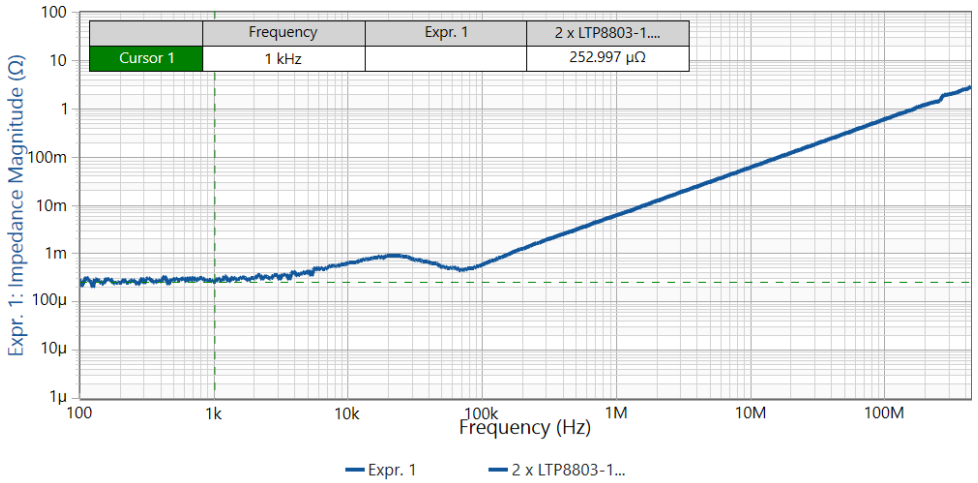

Setup with Bode 500 and
Picotest **P2102A 2-Port Probe**




Setup with Bode 500 and **two**
Picotest **P2104A 1-Port Probes**

# Example of a Lower Impedance




**Picotest 256 A Demo-board** with 2 x LTP8803-1A COT 48V to 1.1Vdc step down regulators.

250 µΩ at 1kHz. Noisy result at low frequency due to non-linear COT control mode.

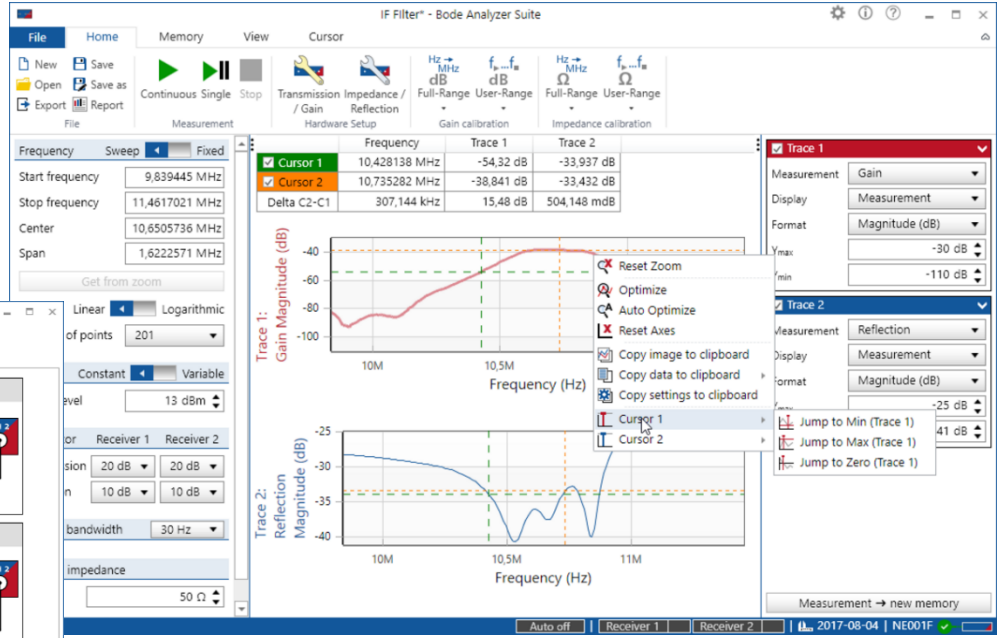
# Key benefits of Bode 500

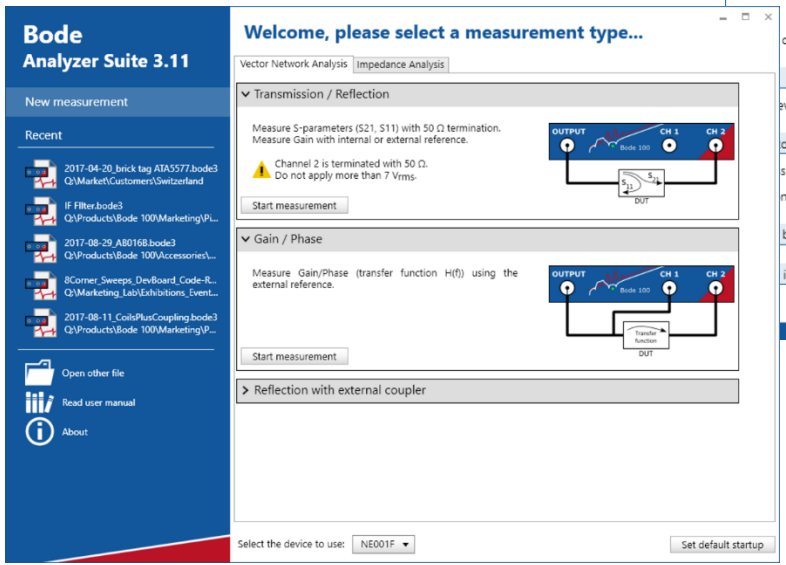
- Frequency Response Analyzer and Vector Network Analyzer in one device
- Reliable results – high accuracy, high dynamic range
- Easy to use – BAS controlled, USB-C, Ethernet
- Portable – compact lightweight design
- 10 mHz to 450 MHz
- Silent



# Bode Analyzer Suite

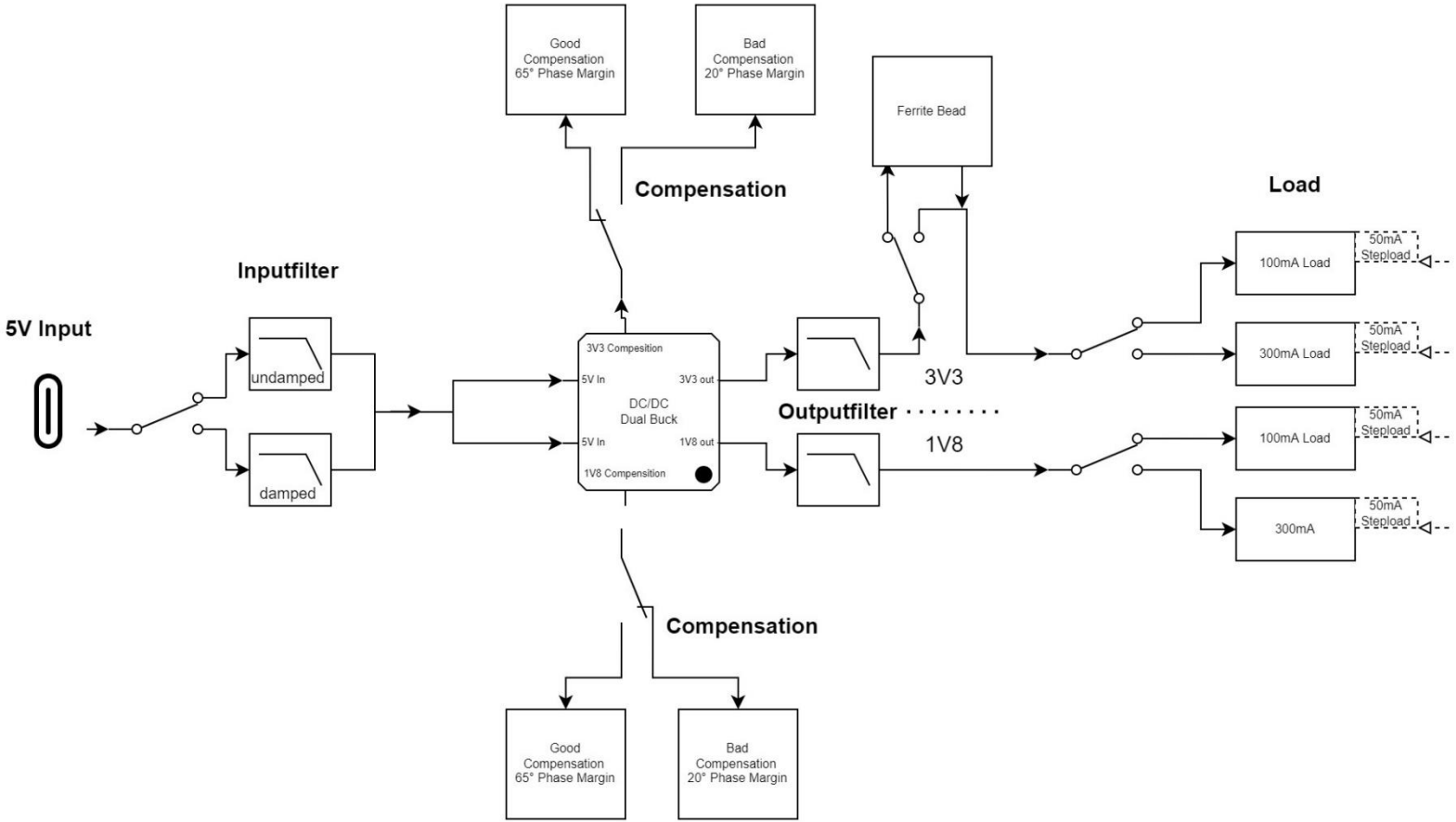
- Easy-to-use
- Powerful
- Free



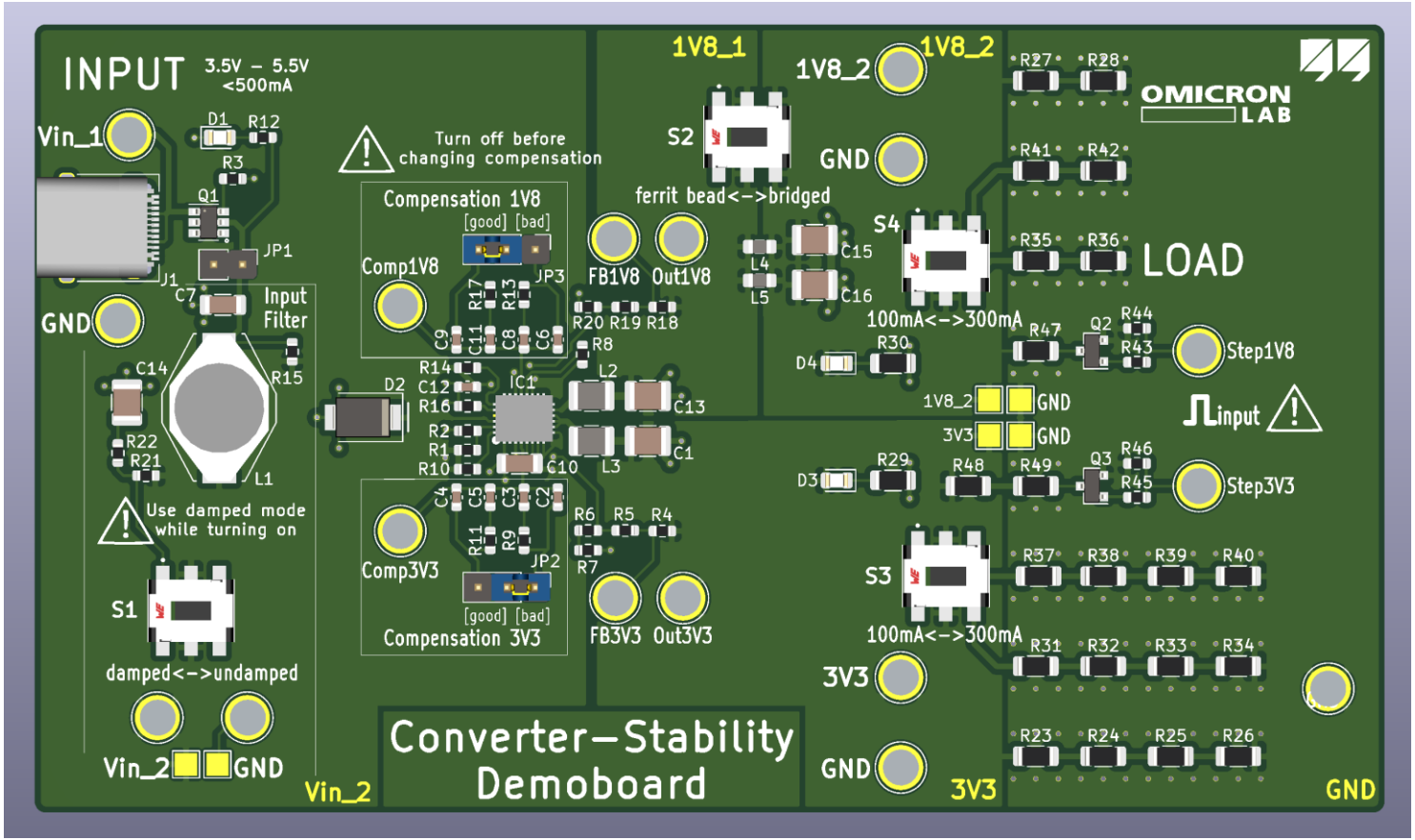




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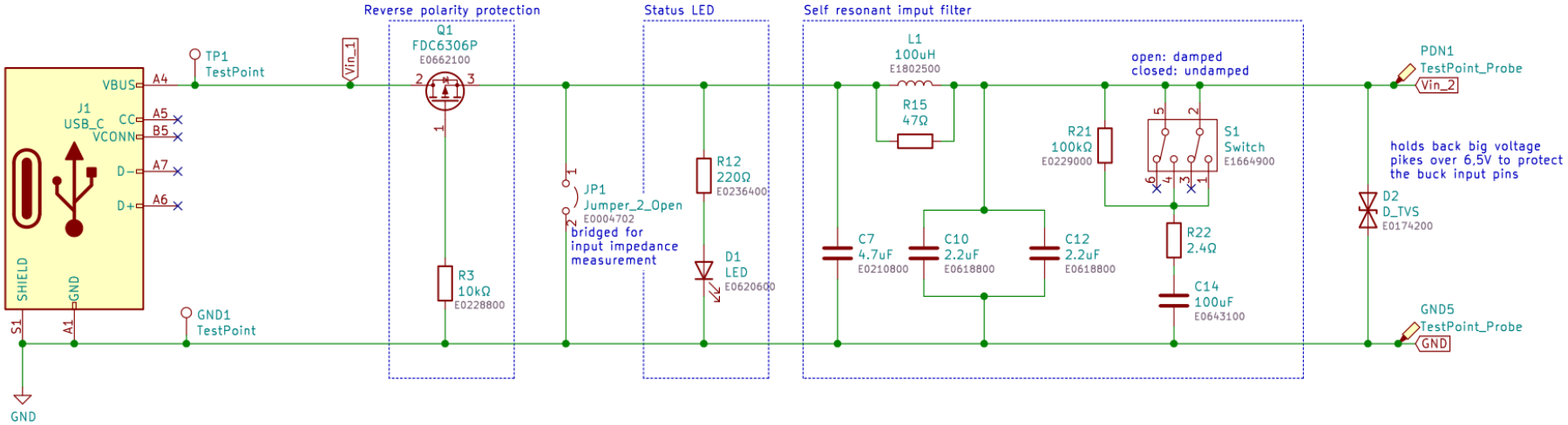
# Hands-On (Converter Stability Demoboard)



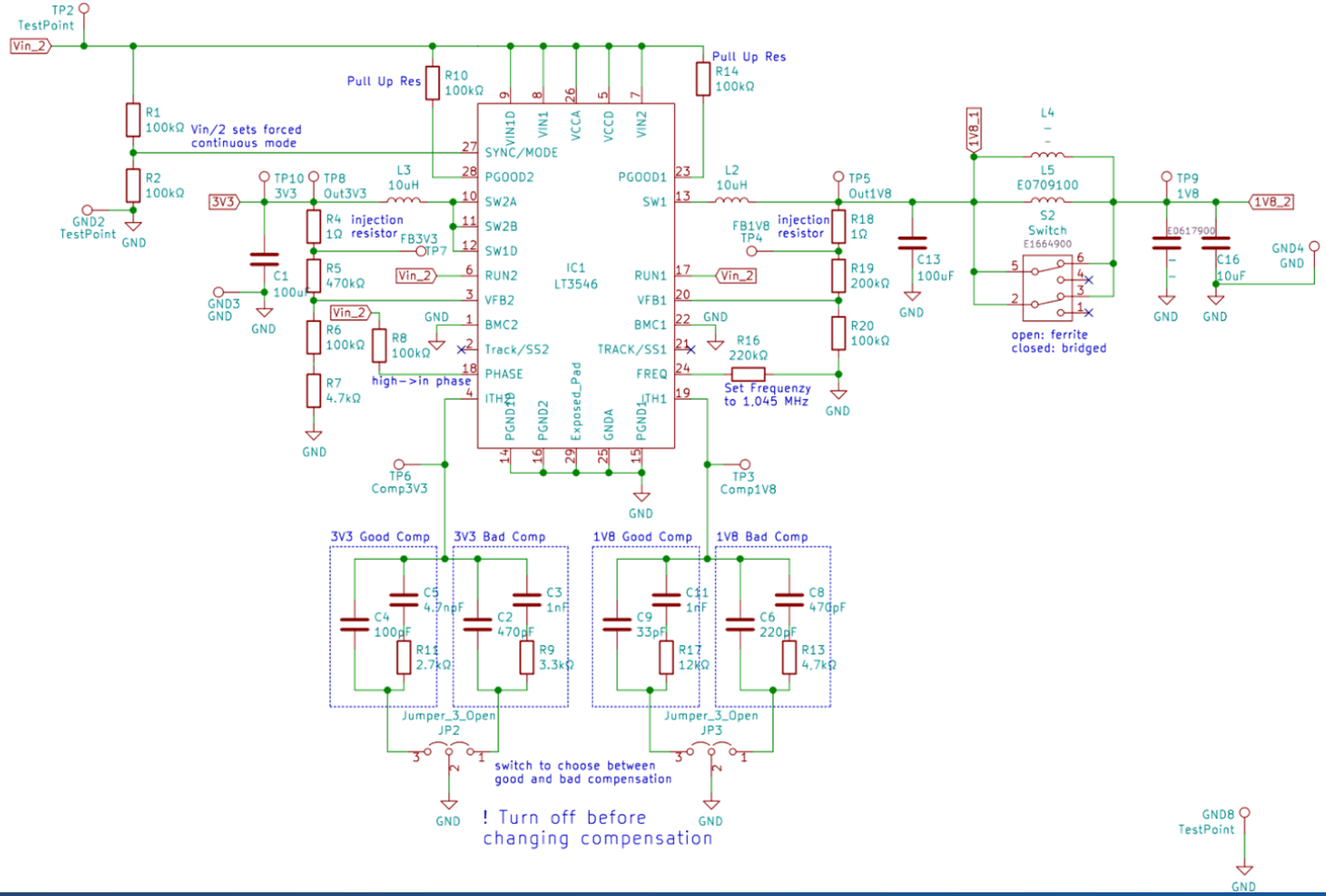
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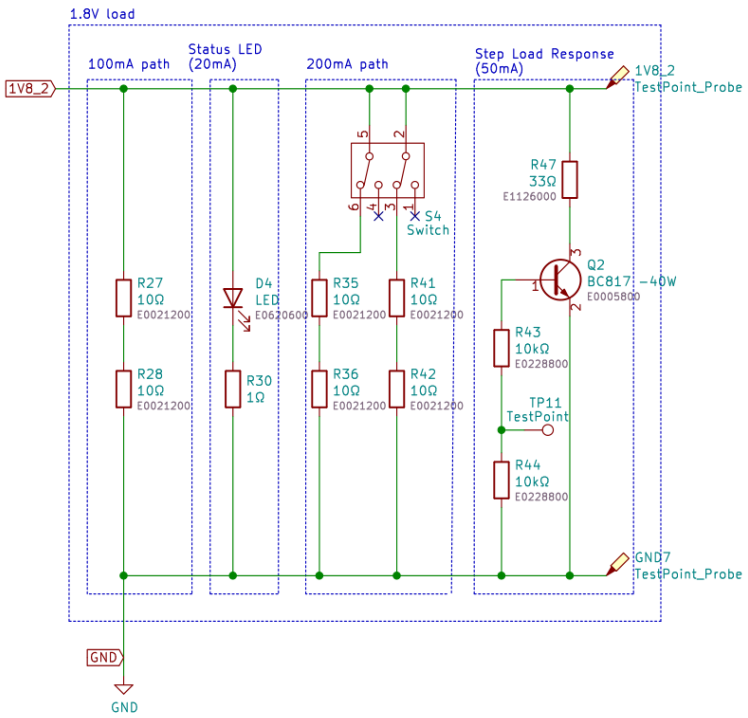
# Input Filter Section

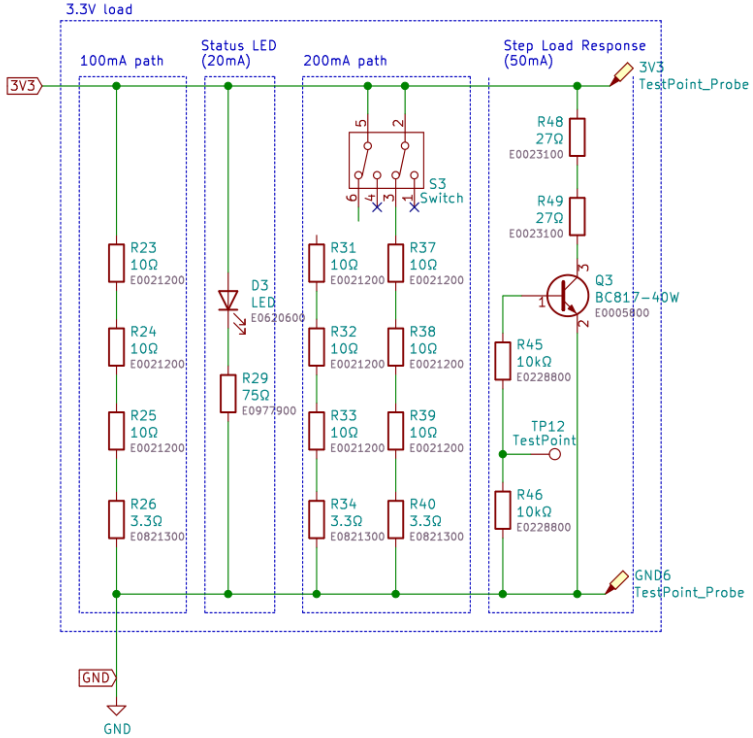


# Dual DC/DC Section

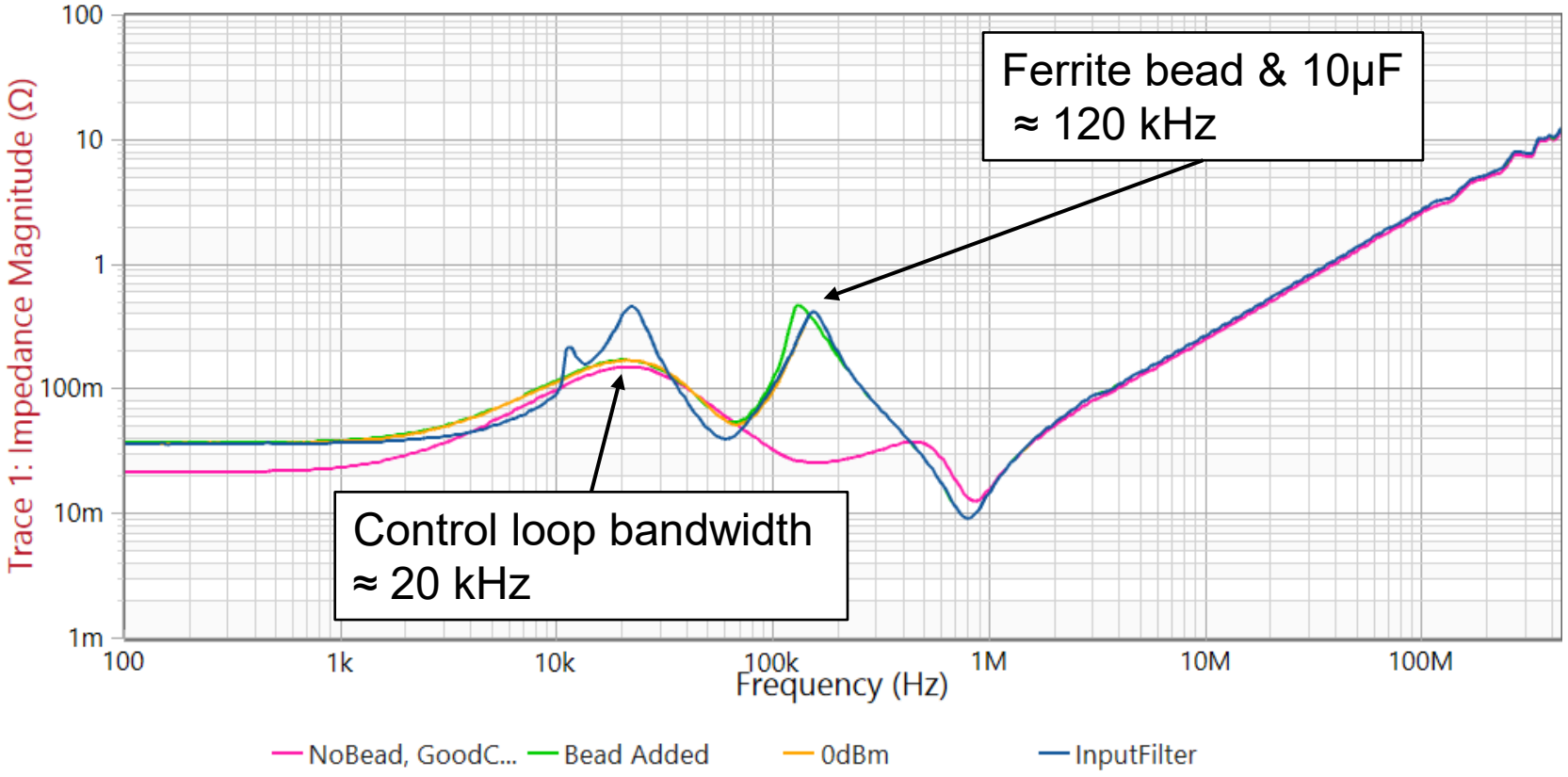


# Load Section



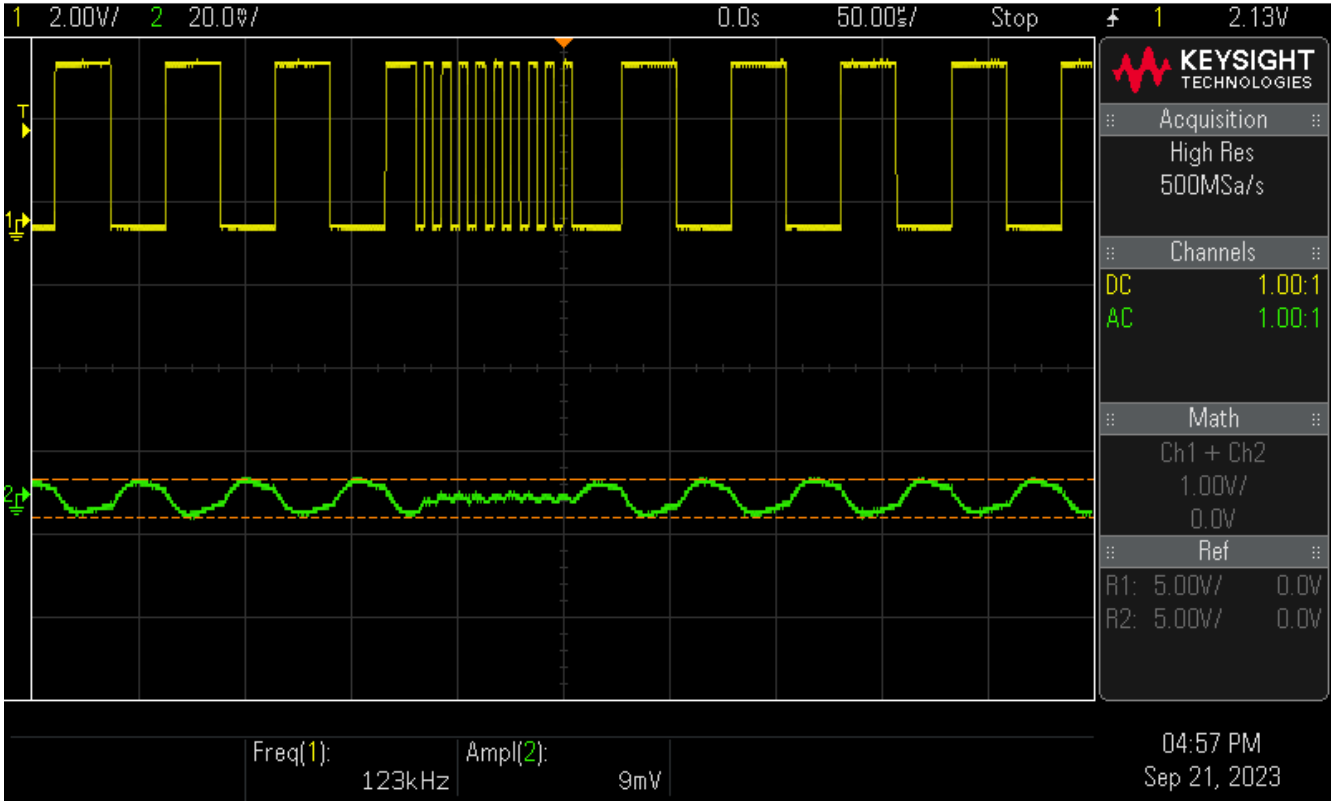



# 1V8 PDN Impedance



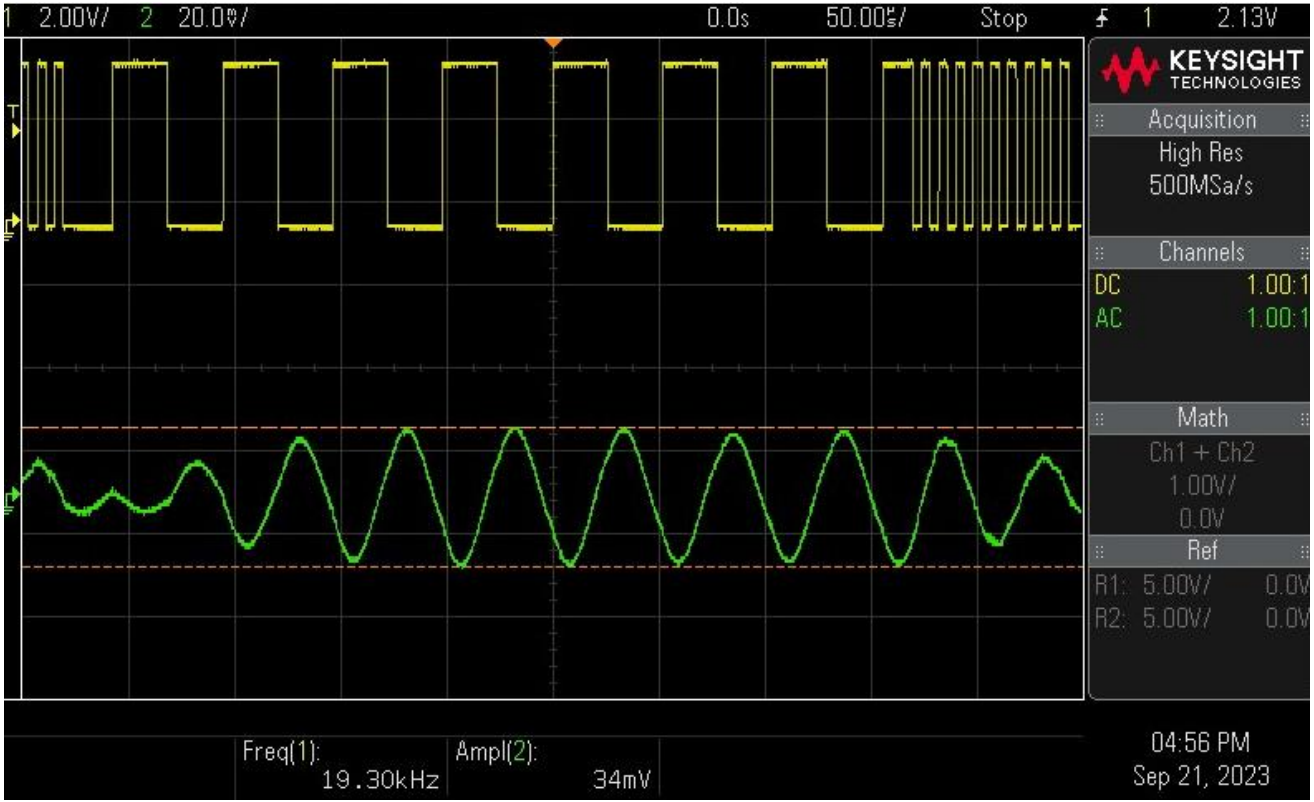
# Load Stepping (20 kHz & 120 kHz)

50° Phase Margin, no 2nd resonance ≈ 9 mVpp



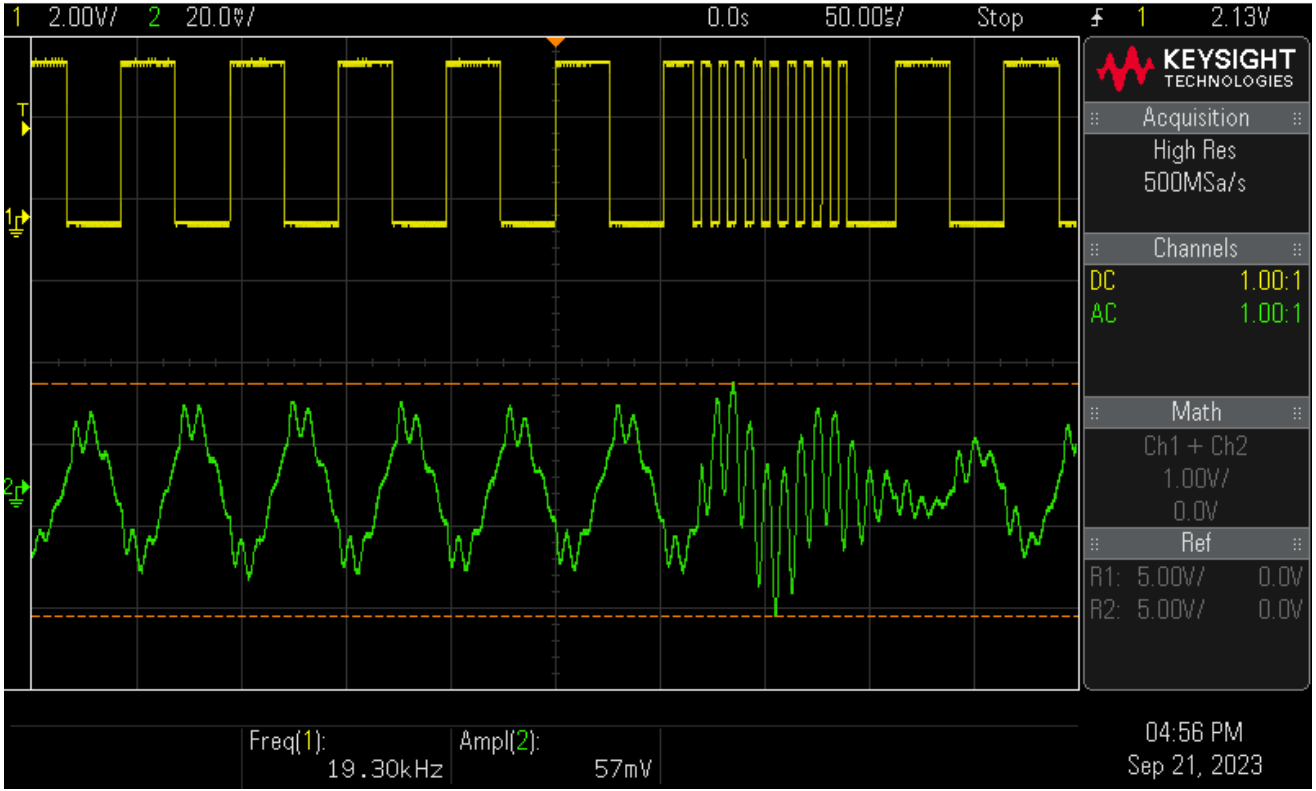
# Load Stepping (20 kHz & 120 kHz)

15° Phase Margin, no 2nd resonance ≈ 34 mVpp



# Load Stepping (20 kHz & 120 kHz)

15° Phase Margin + 2nd resonance ≈ 57 mVpp



# Summary

- PDN impedance reveals information about
  - Control loop stability
  - Resonance frequencies in the PDN network
- Measuring PDN impedance is rather simple
  - The output capacitors are nearly always accessible
  - The control loop must not be broken
- A flat impedance approach guarantees optimum damping at all frequencies
- Lower output impedance results in less noise on power rail




# Thank you for your attention!

If you have questions or proposals to the OMICRON Lab team, please contact us via info@omicron-lab.com.

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