

Keysight Technologies

Signal Integrity Serializer/Deserializer(SERDES) Using Advanced Design System (ADS)

Application Note

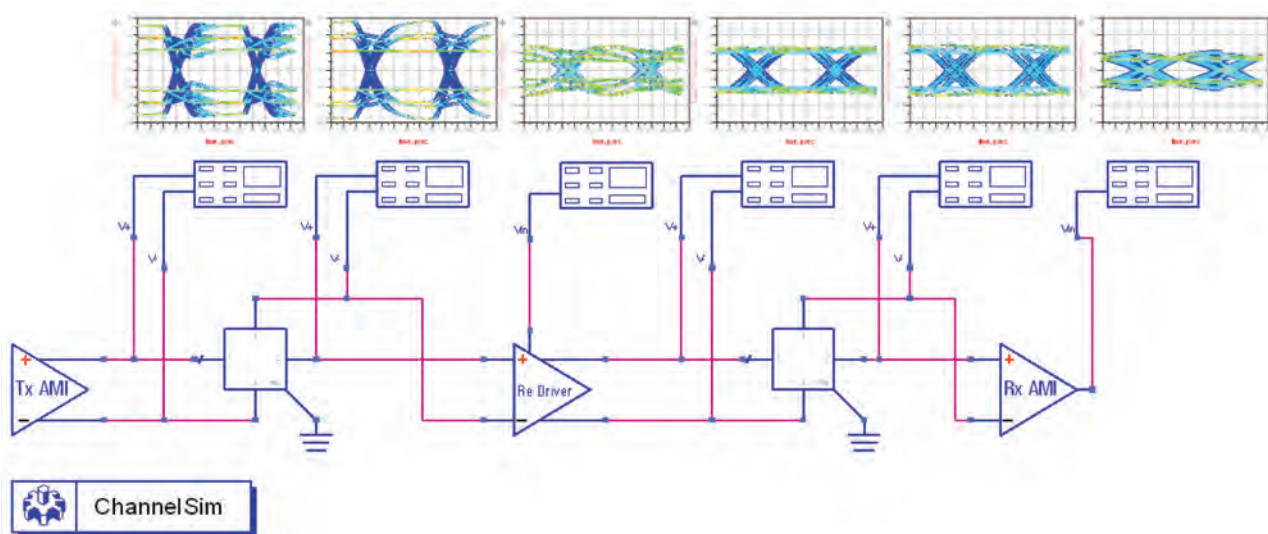


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Question

What are the architectures of the high speed SERDES transmitter and receiver?

Answer

Figure 1 shows the typical physical layer architecture of the SERDES Transmitter (Tx) and Receiver (Rx). Tx includes Encoding, Parallel to Serial, De-emphasis and Differential Driver. Rx includes Differential Receiver, Continuous Time Linear Equalizer (CTLE), Feed Forward Equalizer (FFE), Clock Recovery Circuit, Decision Feedback Equalizer (DFE), Serial to Parallel and Decoding.

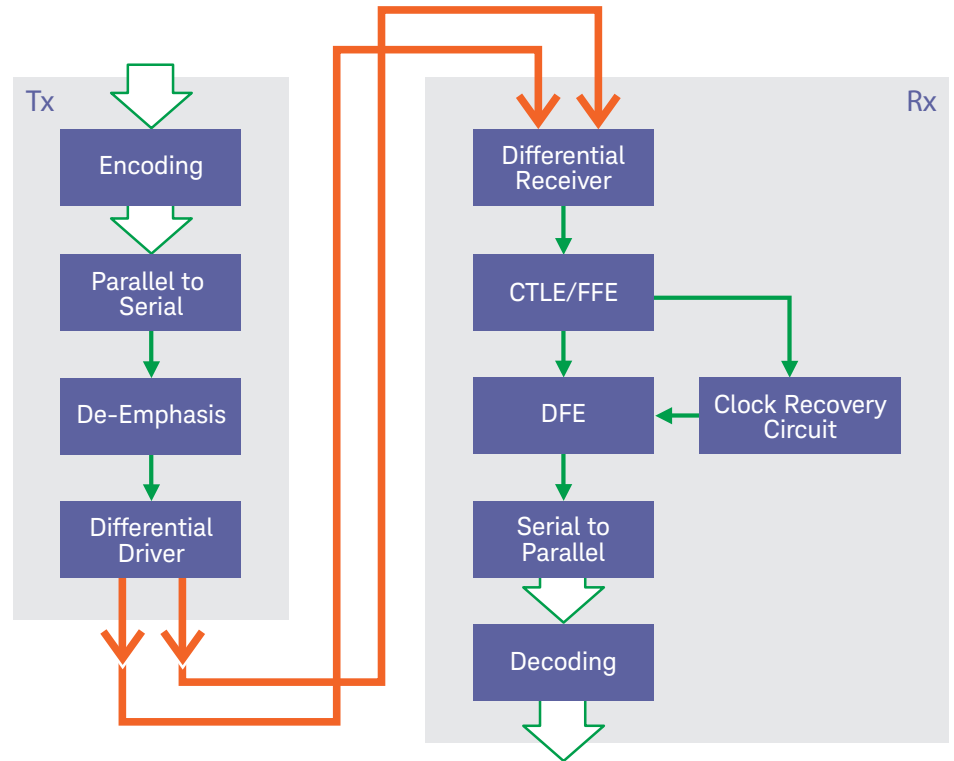
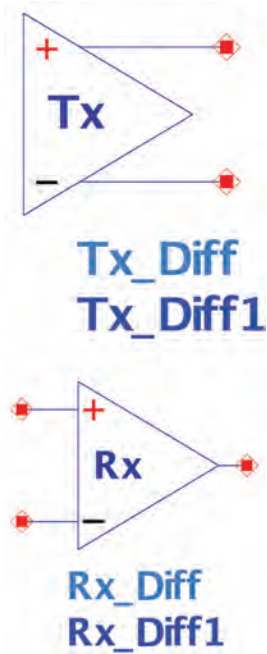


Figure 1. Block diagram of SERDES Tx/Rx architectures.



In ADS, Tx_Diff and Rx_Diff components could be used to model Tx and Rx for high speed SERDES system planning.

In Tx_Diff there are function tabs including:

- Waveform: Bit rate, Vhigh, Vlow and slew rate
- Bit Pattern: LFSR, user defined sequence and bit file
- Encoder: 8b/10b, 64b/66b, 128b/130b and 128b/132b
- EQ: Taps, dB
- Electrical: source impedance
- Jitter: DCD, PJ and RJ

In Rx_Diff there are function tabs including:

- EQ: CTLE, FFE and DFE
- Electrical: load impedance
- Jitter: RJ and amplitude noise

Both FFE and DFE support three adaptive equalization methods as shown in Figure 2.

The three adaptive algorithms are:

- LMS (Least Mean Square)
- RLS (Recursive Least Squares)
- ZF (zero forcing)

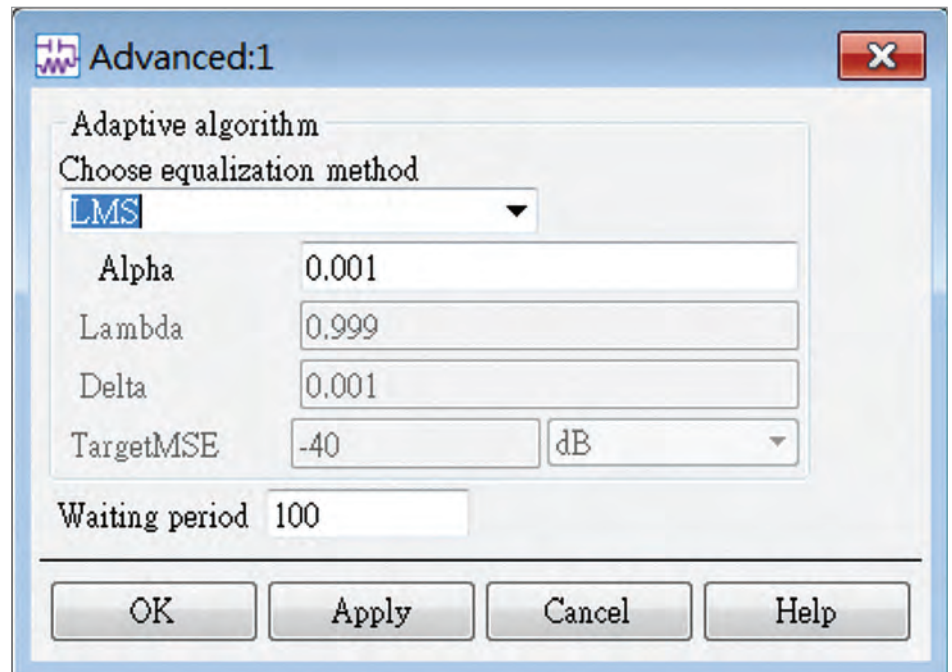


Figure 2. Equalization method setup window.

System level simulation is important when building a high speed SERDES system. Tx_diff and Rx_diff are useful components when planning a high speed SERDES system. We can adjust parameters in Tx_diff/Rx_diff components easily and perform ChannelSim simulation to examine system performance, such as BER and jitter, in minutes.

Question

What is Inter Symbol Interference (ISI)?

Answer

Loss of a transmission line is frequency dependent. In general, loss increases as frequency increases. Conductor loss and dielectric loss of substrate are main contributors to loss of a transmission line. To estimate the loss of a transmission line, we can assign material properties of substrate and physical size of a transmission line as shown in Figure 3. By performing an S-Parameter simulation we will get insertion loss versus frequency as shown in Figure 4.

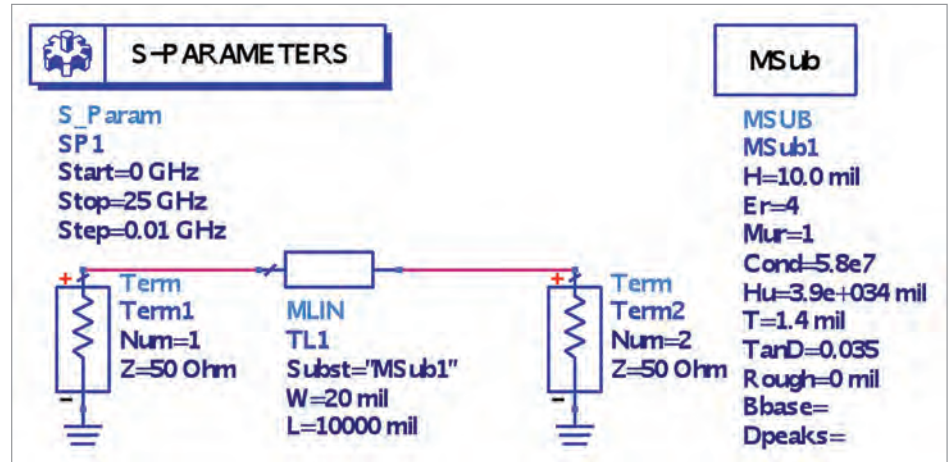


Figure 3. Insertion loss simulation of a transmission line.

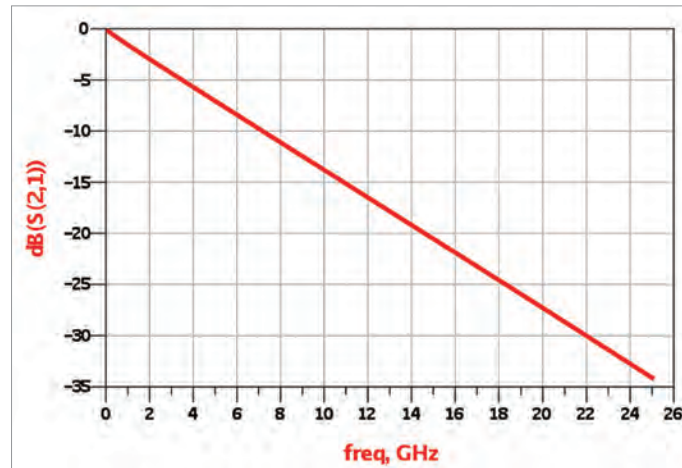


Figure 4. Frequency dependent insertion loss of a transmission line.

We excite a 100ps impulse to a transmission line as shown in Figure 5. In Figure 6, the left diagram shows the slew rate of the output impulse response becoming slower. Compare the spectrum of impulse with impulse response and we can see that loss of high frequency components of the impulse response is greater than the loss of low frequency components as shown in the right diagram of Figure 6.

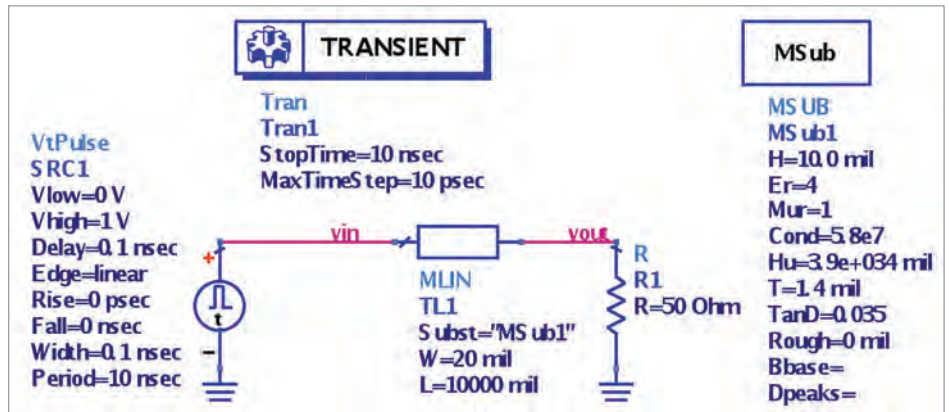


Figure 5. Impulse response simulation.

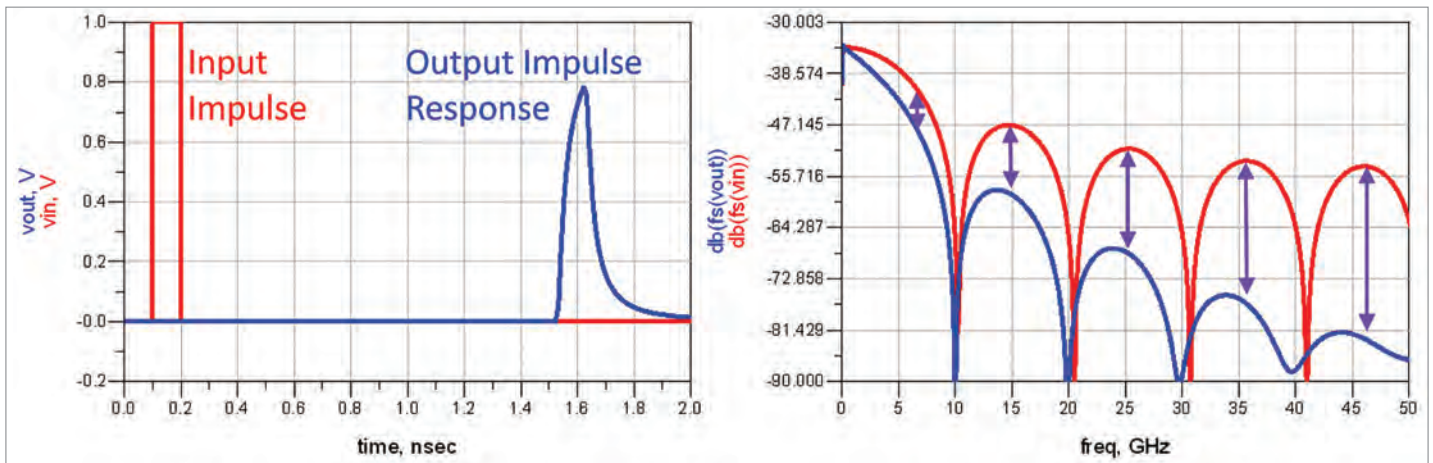


Figure 6. Impulse/impulse response (left) and their spectrum (right).

Label one Unit Interval (UI) on the output impulse response. The center of the symbol could be at the peak of the symbol as shown in Figure 7. We can then find that interference labeled in red regions penetrating to adjacent symbols. It explains what Inter-Symbol-Interference means. ISI is the most critical factor impacting performance of a SERDES design.

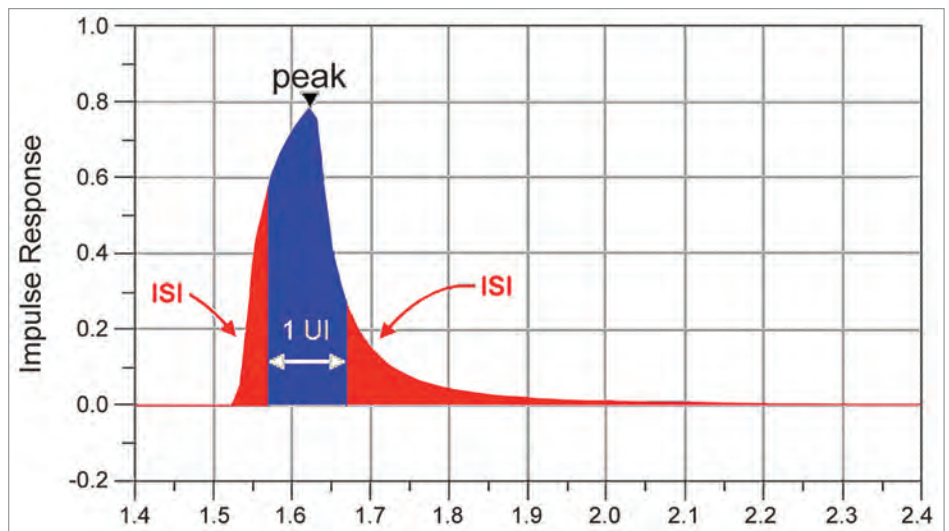


Figure 7. Interference penetrating to adjacent symbols.

Question

How does pre-emphasis work to improve a high speed digital signal?

Answer

When a high speed digital signal travels through a lossy channel, the signal edges deteriorate with the loss of high frequency signal components as shown in the right diagram of Figure 8. It results in inter-symbol-interference (ISI) and a closing eye. One way to mitigate high frequency loss is to use a pre-emphasis circuit in the transmitter (TX). A pre-emphasis circuit operates by boosting high frequency energy every time a transition occurs as shown in left diagram of Figure 9. It compensates high frequency loss of a signal at the receiver (RX) and improves signal quality as shown in the right diagram of Figure 9.

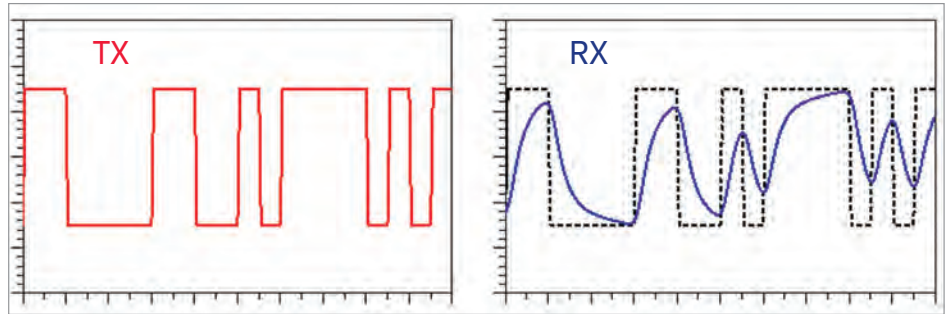


Figure 8. High frequency loss results in signal deterioration at RX.

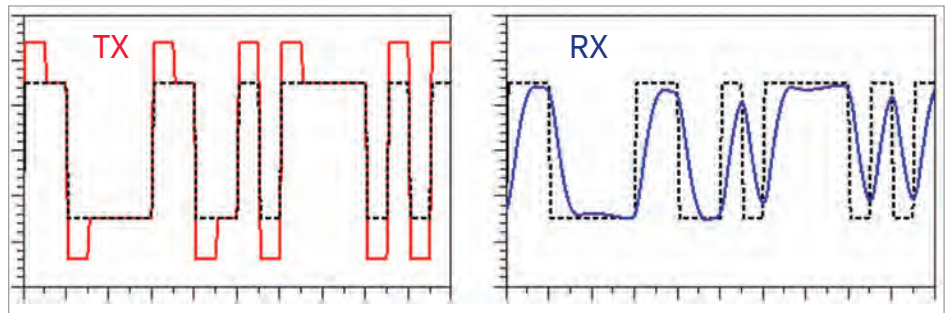


Figure 9. High frequency compensation with pre-emphasis.

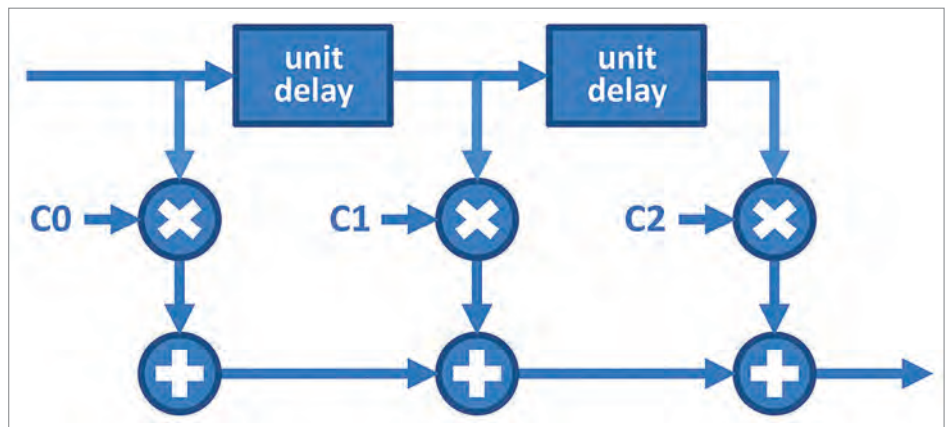


Figure 10. Three taps pre-emphasis circuit architecture.

A pre-emphasis circuit can be constructed from a multi-taps finite impulse response (FIR) filter as shown in Figure 10. We can set up tap values (C0, C1, C2) to adjust boosting levels. In ADS, Tx_Diff and Tx_SingleEnded components allow users to input tap values as shown in Figure 11. Figure 12 shows eye diagrams with pre-emphasis disabled and pre-emphasis enabled. We can see that the eye of the signal improves with pre-emphasis.

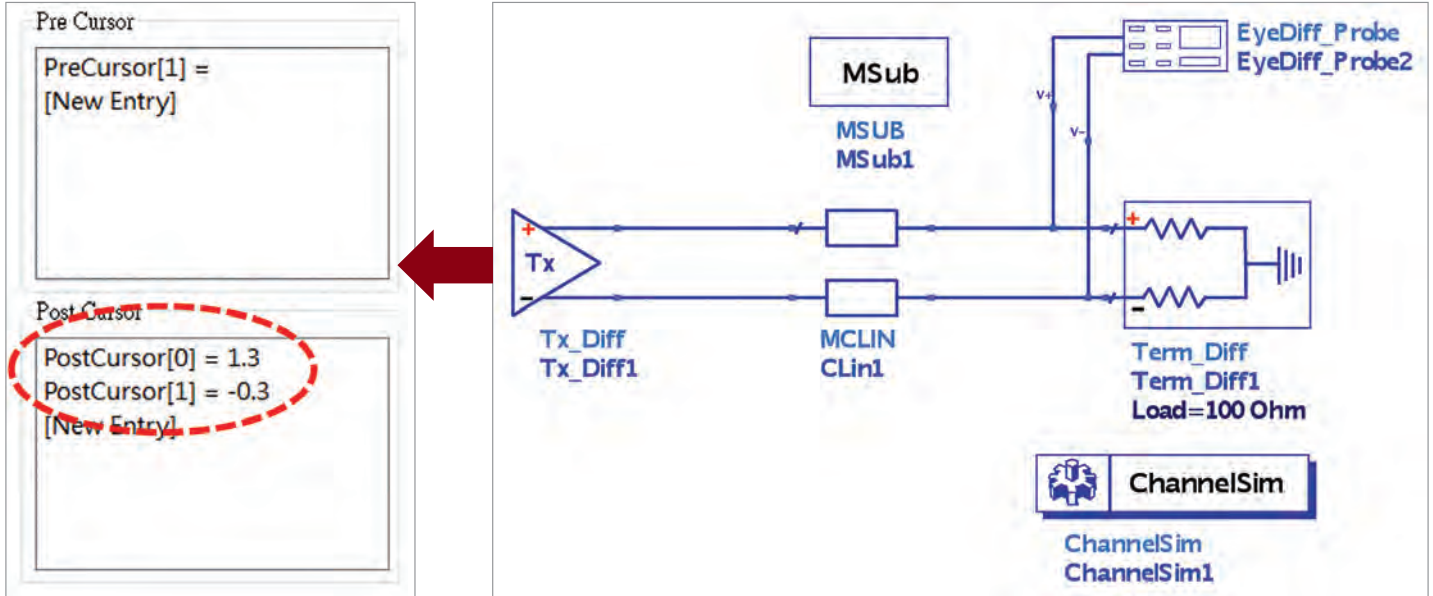


Figure 11. Set up pre-emphasis in Tx_Diff component.

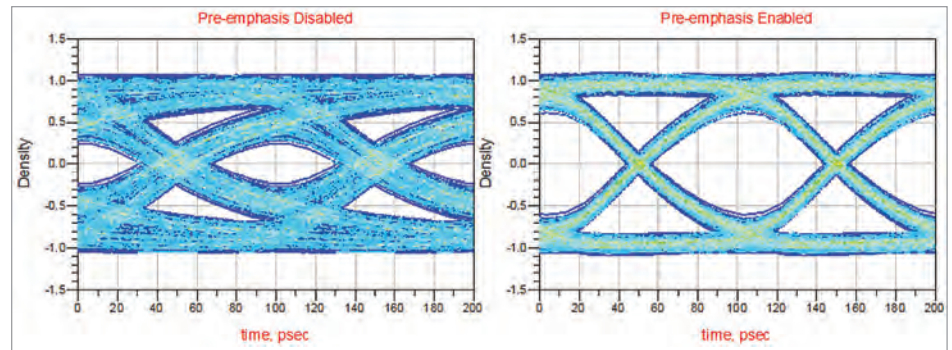


Figure 12. Pre-emphasis disabled (left) and pre-emphasis enabled (right).

Question

How does Continuous Time Linear Equalizer (CTLE) work to improve a high speed digital signal?

Answer

CTLE is an analog filter in a receiver (RX). It could be an active or a passive circuit. When a high speed digital signal propagates through a lossy channel, RX CTLE is used to boost high frequency components of the signal to compensate high frequency channel loss. We used to model behavior of a CTLE by a transfer function. For example, the transfer function of USB3.0 CTLE for a long channel is:

$$H(s) = \frac{A_{dc}\omega_{p1}\omega_{p2}}{\omega_z} \cdot \frac{s + \omega_z}{(s + \omega_{p1})(s + \omega_{p2})}$$

Where

$$A_{dc} = 0.667$$

$$\omega_z = 2\pi \times 650\text{MHz}$$

$$\omega_{p1} = 2\pi \times 1.95\text{GHz}$$

$$\omega_{p2} = 2\pi \times 5\text{GHz}$$

Figure 13 shows the transfer function of the CTLE:

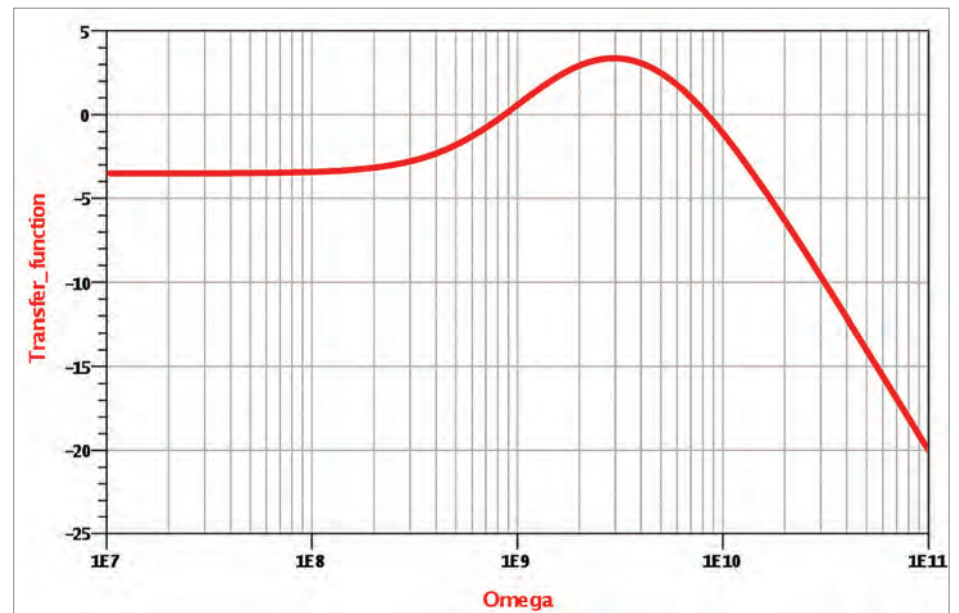


Figure 13. Transfer function of USB3.0 CTLE for long channel.

Figure 14 shows the step response of the CTLE. We can see that the signal level at the transition edge is boosted by CTLE. In ADS, Rx_Diff and Rx_SingleEnded components allow users to input poles and zeros of the CTLE transfer function as shown in Figure 15. Figure 16 (left) shows the eye with CTLE disabled. Figure 16 (right) shows the eye with CTLE enabled. We can see that the eye of the signal is improved with CTLE.

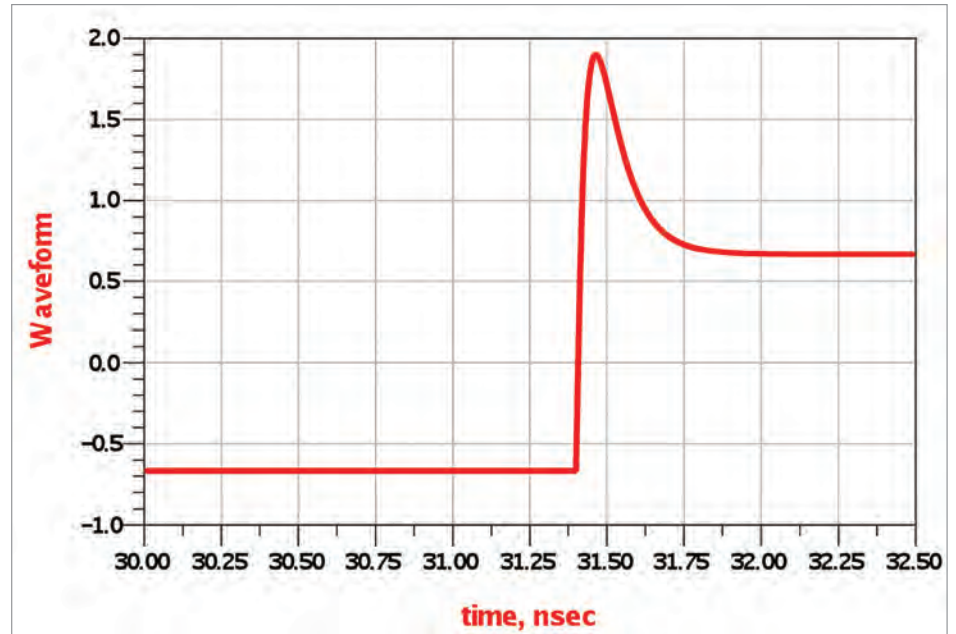


Figure 14. Step response of the CTLE.

Pole/Zero:13

Zeros

Zero[1] = $-2 \cdot \pi \cdot 650e6$
[New Entry]

Poles

Pole[1] = $-2 \cdot \pi \cdot 1.95e9$
Pole[2] = $-2 \cdot \pi \cdot 5e9$
[New Entry]

Pre-factor $2 \cdot \pi \cdot 10.005e9$

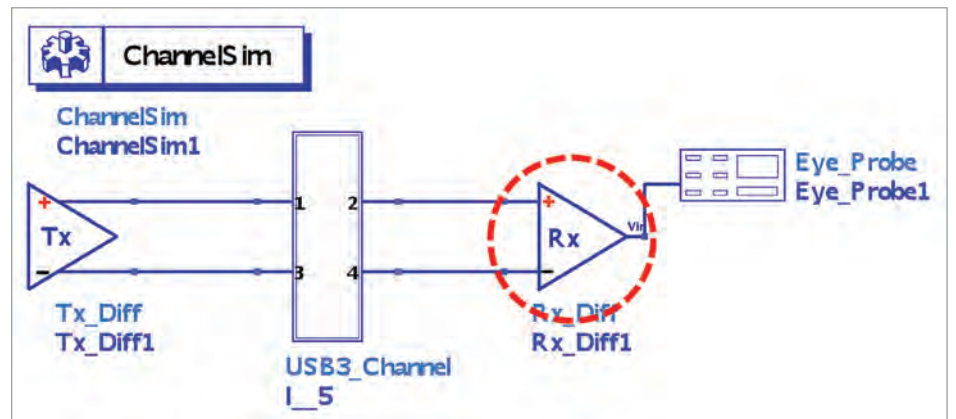


Figure 15. Set-up poles and zeros of the CTLE transfer function.

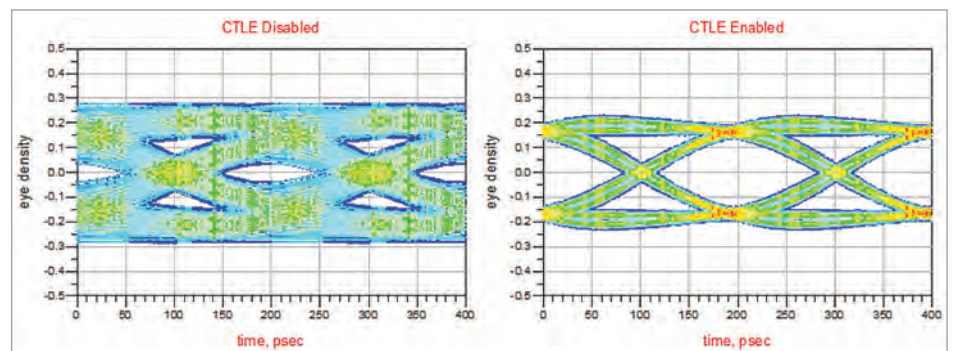


Figure 16. Eyes with CTLE disabled (left) and CTLE enabled (right).

Question

How does Feed Forward Equalizer (FFE) work to improve a high speed digital signal?

Answer

An FFE is a tapped delay line circuit that produces a delayed and weighted sum of an input signal. FFE is widely used in a SERDES receiver (RX) to mitigate Inter-Symbol-Interference (ISI) caused by a lossy channel. Figure 17 shows a three-taps FFE example. Tap values C_0 , C_1 and C_2 are optimized to minimize ISI.

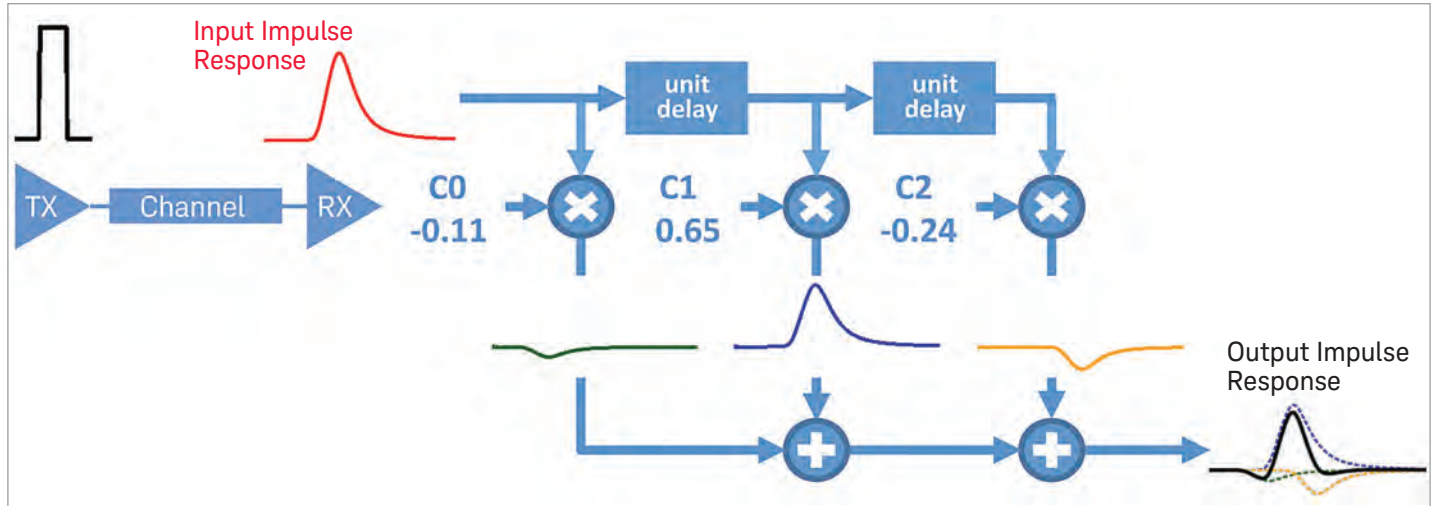


Figure 17. A three taps FFE example.

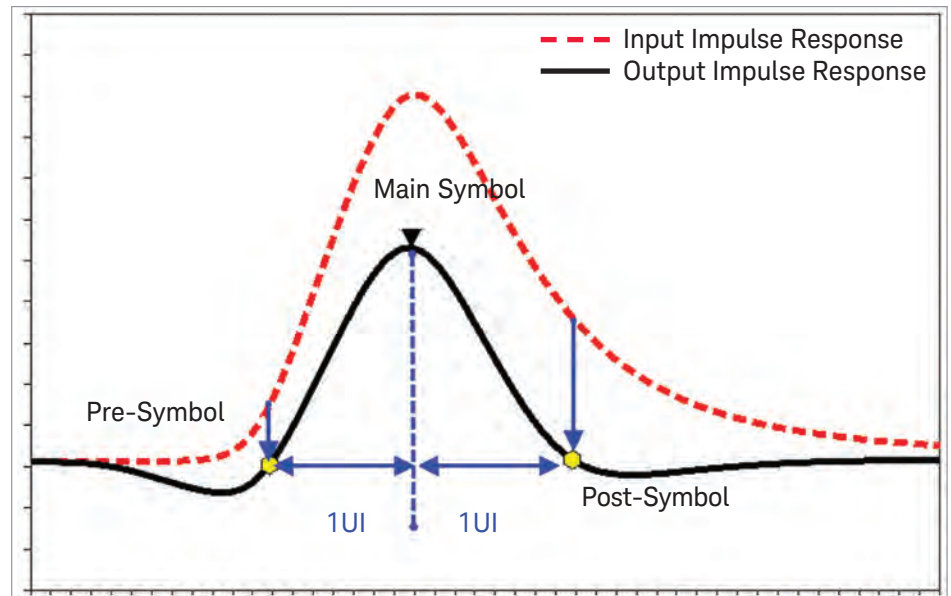


Figure 18. Output impulse response of FFE has zero interference at pre-symbol and post-symbol sampling points.

In this example, tap values are -0.11, 0.65 and -0.24. The first tap is used to minimize pre-ISI. The second tap is used to adjust the main signal level. The third tap is used to minimize post-ISI. Note that tap values here are normalized, where $|C0|+|C1|+|C2|=1$. The output impulse response of the DFE has zero interference at sampling points of the pre-symbol and post-symbol as shown in Figure 18.

In a channel simulation as shown in Figure 19, Rx_SingleEnded and Rx_Diff components allow users to enable “optimized initial tap calculations” as shown in Figure 20. When the simulation ends, optimal tap values will be written into a text file. Figure 21 (left) shows the eye patterns of FFE disabled and Figure 21 (right) shows the eye pattern with FFE enabled. We can see that the eye pattern is improved with FFE.

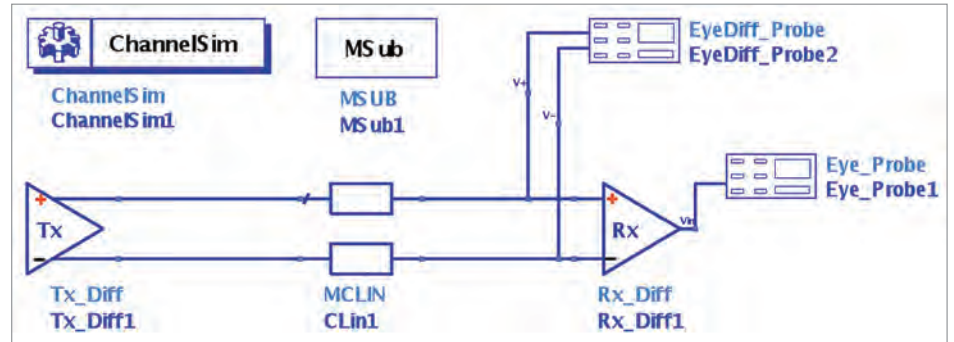


Figure 19. A Channel Simulation.

```

taps.txt
1 PreCursor
2 -0.11
3 PostCursor
4 0.65
5 -0.24
    
```

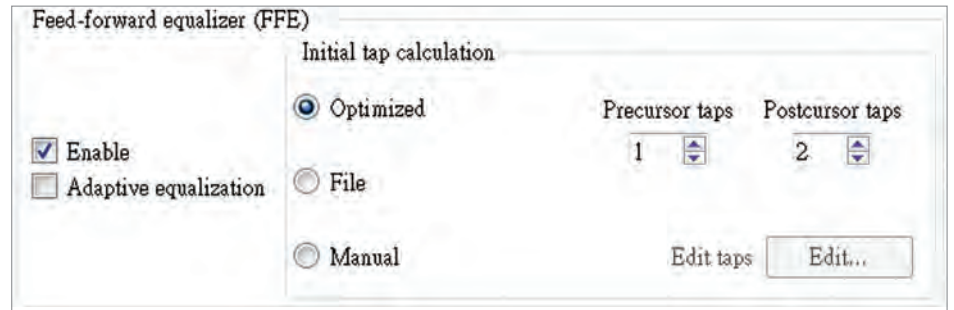


Figure 20. Enable optimization for tap values of the FFE

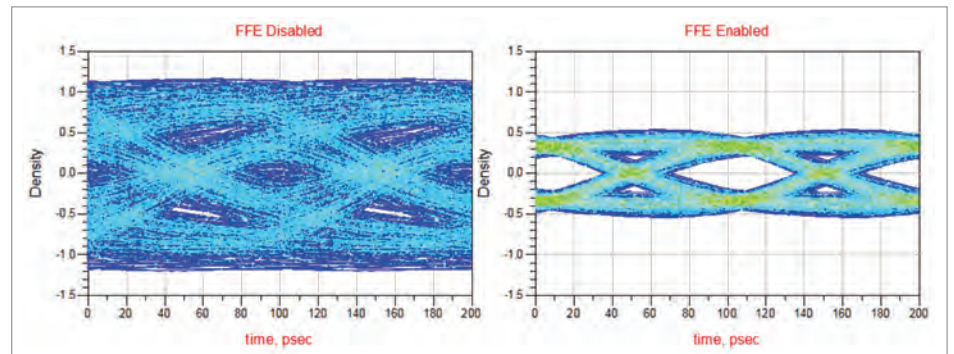


Figure 21. Eye with FFE disabled (left) Eye with FFE Enabled (right).

Question

How does a Decision Feedback Equalizer (DFE) work to improve a high speed digital signal?

Answer

DFE is commonly used in a SERDES receiver (RX) to remove Inter Symbol Interference (ISI) caused by a lossy channel. A DFE includes a Finite Impulse Response (FIR) filter, a summer and a slicer for symbol decision. Figure 22 shows a three taps DFE example. The benefit of a DFE is that it can cancel the ISI without noise amplification. The downside is that it can't correct a precursor ISI.

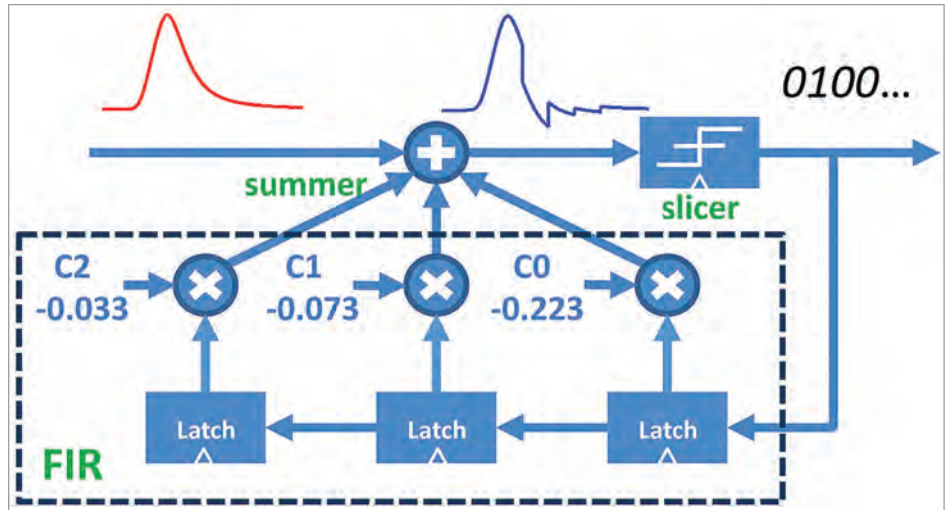


Figure 22. A three taps DFE example.

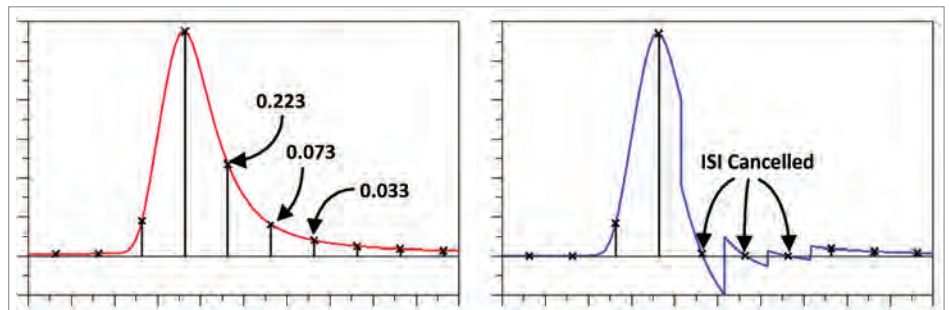


Figure 23. Input impulse (left), output impulse response (right).

First, ISI from the previous symbols are calculated with FIR. The interference is then subtracted from the incoming signal. Finally, the slicer makes a symbol decision and outputs the symbol back to FIR. Tap values are selected to minimize ISI. In this example, tap values are -0.223, -0.073 and -0.033. Figure 23 shows that interference at sampling points of post symbols are removed.

In a channel simulation as shown in Figure 24, Rx_SingleEnded and Rx_Diff components allow users to enable “optimized initial tap calculations” for DFE as shown in Figure 25. When the simulation ends, optimal tap values will be written into a text file. The left image in Figure 26 shows eye patterns of DFE disabled and the right image shows eye pattern with DFE enabled. We can see that eye pattern was improved with DFE.

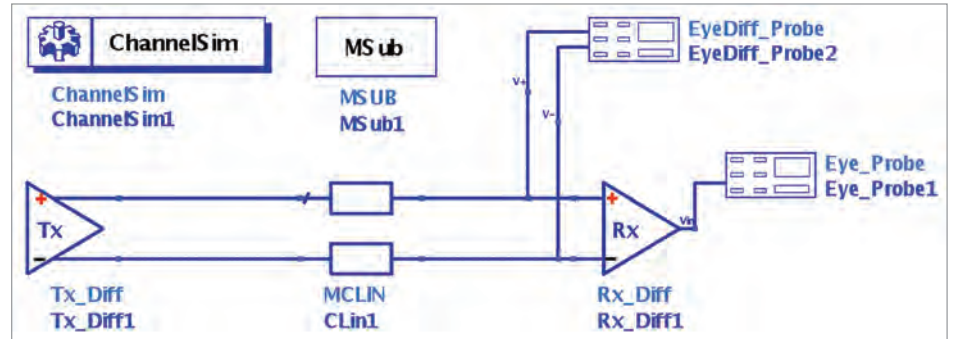


Figure 24. A Channel Simulation.

taps.txt	
1	DFETap
2	-0.223
3	-0.073
4	-0.033

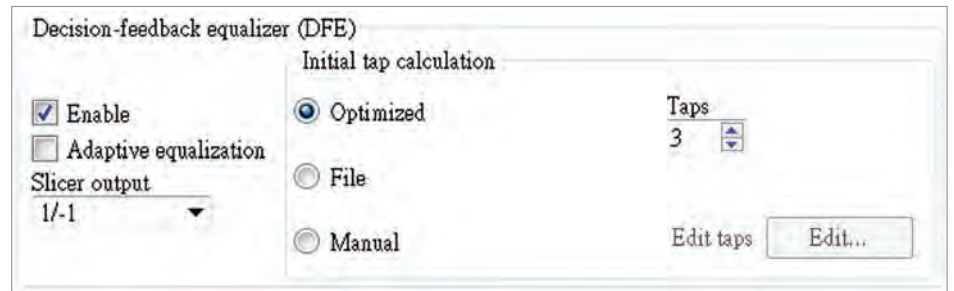


Figure 25. Enable optimal DFE taps calculation.

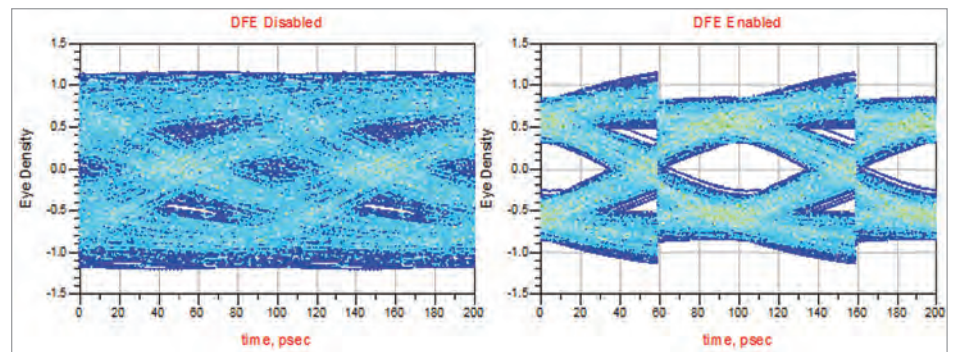



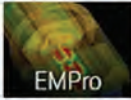
Figure 26. Eye with DFE disabled (left), Eye with DFE Enabled (right).

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Advanced Design System (ADS)

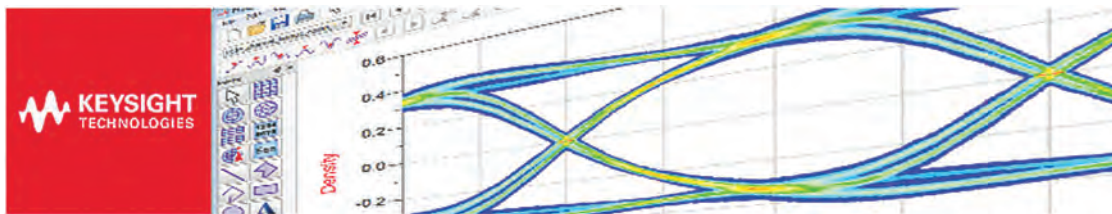


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Category: ADS (ADS Tips)

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1939

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