APPLICATION NOTE

How to Detect Signal Integrity Issues in Chiplet Designs Early

KEYSIGHT

Introduction

Chiplet design represents a new era in the semiconductor design process, promising enhanced performance, cost efficiency, and scalability. However, this innovative approach also brings unique signal integrity (SI) challenges that necessitate standards for reliable operation and future compatibility.

This application note covers:

- The rise of the chiplet design philosophy
- Signal integrity (SI) complexities in chiplet designs
- SI specifications for the electrical layers from the Universal Chiplet Interconnect Express (UCIe) standard
- Leveraging Electronic Design Automation (EDA) tools to overcome these chiplet design challenges.

Rise of Chiplet Designs

The shift towards chiplet design is a practical response to the need for cost-effective, low-risk semiconductor manufacturing processes [1].

In the conventional monolithic approach, achieving better performance requires a larger die size. In contrast, chiplet-based design, as depicted in Figure 1, strategically separates different functions into individual smaller dies. This approach enhances cost efficiency, yield, and scalability. The term 'chiplet' denotes the compact size of each die/chip.

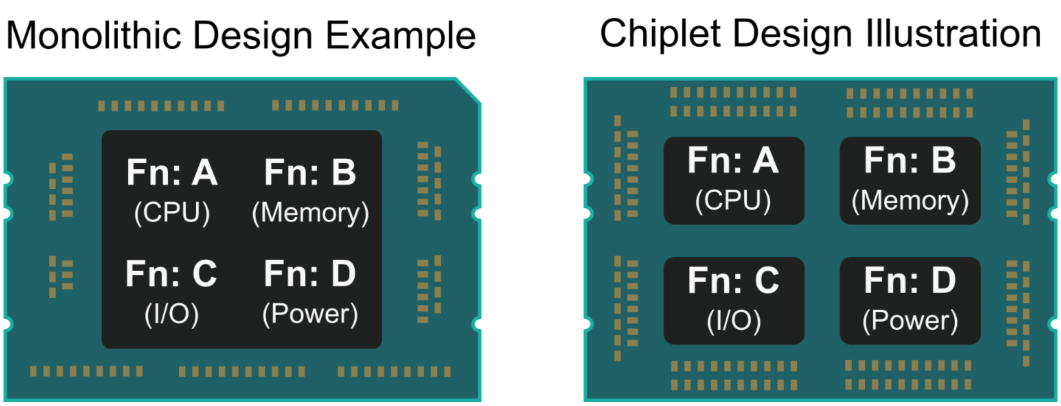

Figure 1. Comparison between the monolithic chip design and chiplet design approach. Chiplet designs have smaller die sizes to increase cost efficiency, yield, and scalability.

Cost and yield

In practice, manufacturing the entirety of a larger chip design with the most advanced technology (advanced node) can cost almost twice as much as the chiplet approach [2]. Also, not all functions within a large design necessitate fabrication with the most advanced technology.

Monolithic designs require larger die (reticle) sizes to increase computational power. This increase in size introduces two problems:

- The large reticle size can reach the fabrication limit
- The yield of the large reticle size can be too low to be profitable

Figure 2 and Figure 3 compares the two design approaches using wafers of the same size and four similar defects. Consider the example where a large monolithic chip requires four functional blocks—A, B, C, and D—to work. As illustrated in Figure 2, defects in functions A, B, C, or D on the same die render the entire die unusable. The yield for a monolithic approach is 66.7%.

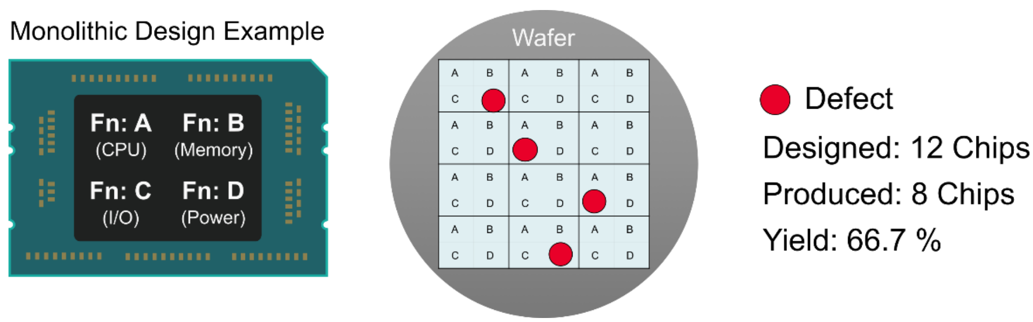

Figure 2. Given four defects on a wafer with 12 chip-designs, only eight chips will be usable. The yield is 66.7%.

On the other hand, because the chiplet design splits the chip functions into four smaller dies, if one defect is found on A, only the die with the particular function A is impacted, not the entire chip (A, B, C, and D). In this case, the yield can be as high as 97.3% with the same four defects, as shown in Figure 3.

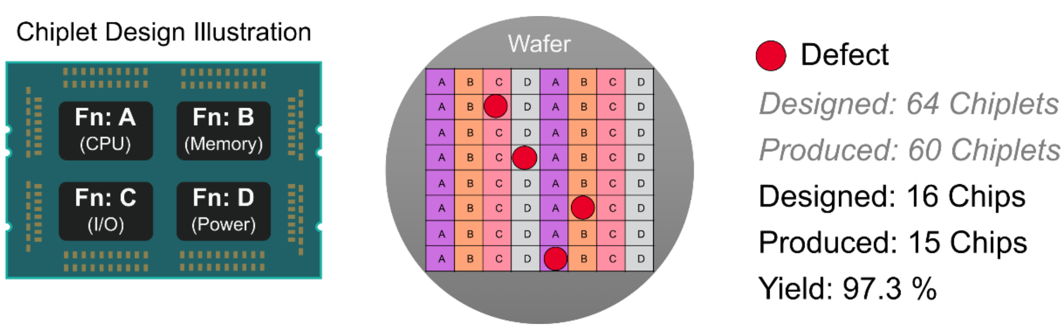

Figure 3. Given the same four defects, the wafer with chiplet designs reaches a higher yield because of the smaller dies and modular design.

Signal Integrity Challenges in Chiplet Designs

Having discussed the cost and yield benefits, we now address the signal integrity challenges in chiplet designs. Although the chiplet's modular approach increases yield, the functional blocks are now on different dies. This introduces:

- Increased design complexity
- Challenges in chiplet die-to-die (D2D) communication

As a result, robust signal integrity analysis of the D2D communication is crucial in establishing the reliability and interoperability of chiplet-based designs. Key components of D2D signal integrity (SI) include the following.

Loss

The frequency-dependent loss from D2D interconnects attenuates high-frequency components more than lower-frequency ones. As shown in Figure 4, this low-pass behavior of the interconnect alters the frequency spectrum of the input data, causing rise time degradation.

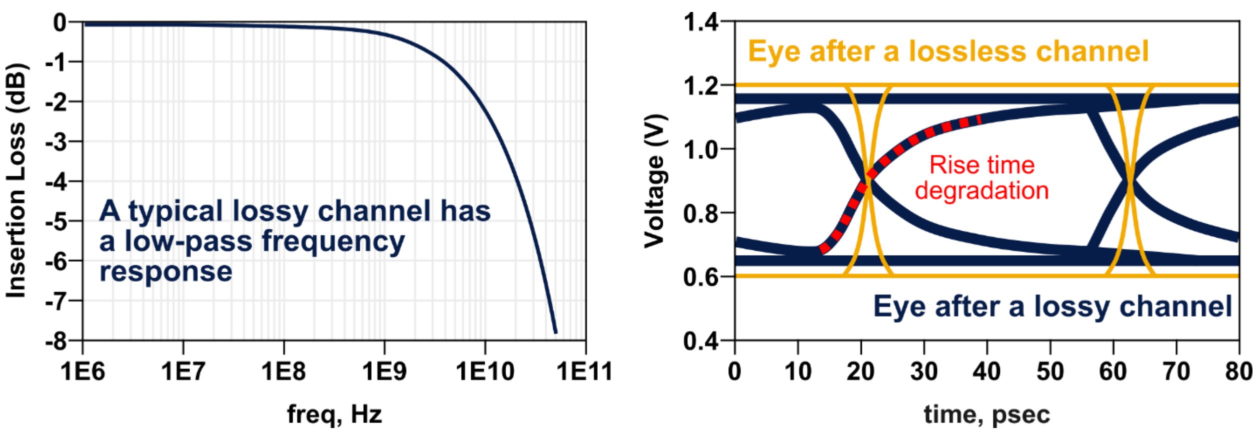

Figure 4. Left: A typical interconnect has a low-pass frequency response. Right: The low-pass frequency response causes rise time degradation. The degradation manifests in the edge transition of the eye diagram, indicated by the red dotted line.

Crosstalk

As the interconnect density increases and signal traces are closer to each other, crosstalk becomes a primary signal integrity concern. Because of the interconnect's physical proximity, the energy in adjacent interconnects can couple into the line of interest. As shown in Figure 5, the crosstalk noise appears in the received eye as peaks in the transition region.

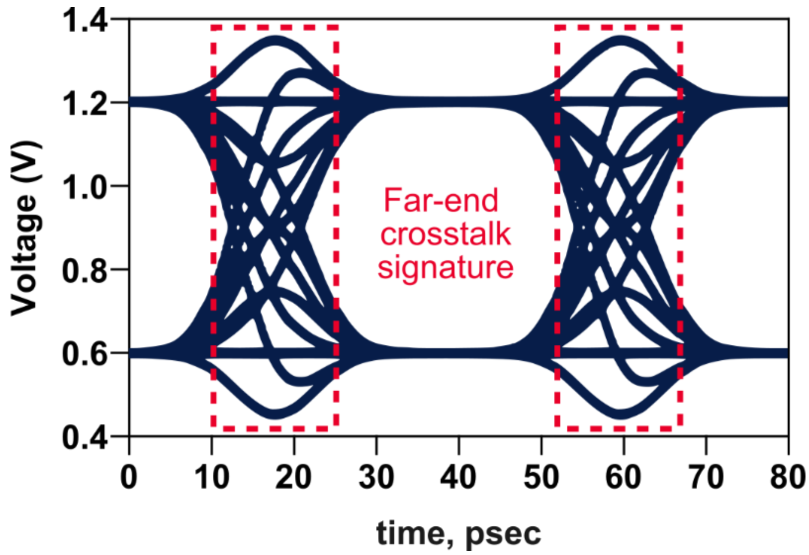

Figure 5. The energy of close-by signal lines (aggressors) can couple into the data line of interest (victim), causing peaking in the transition area of the eye diagram, indicated by red dotted rectangles.

Transmitter and receiver configuration

As the optimization of the interconnect design reaches the final stages, one looks to the transmitter (Tx) and receiver (Rx) to further improve the signal integrity. Termination strategies and equalization techniques can be applied to the transmitter and receivers. Figure 6 shows an example of a Tx eye diagram after applying de-emphasis.

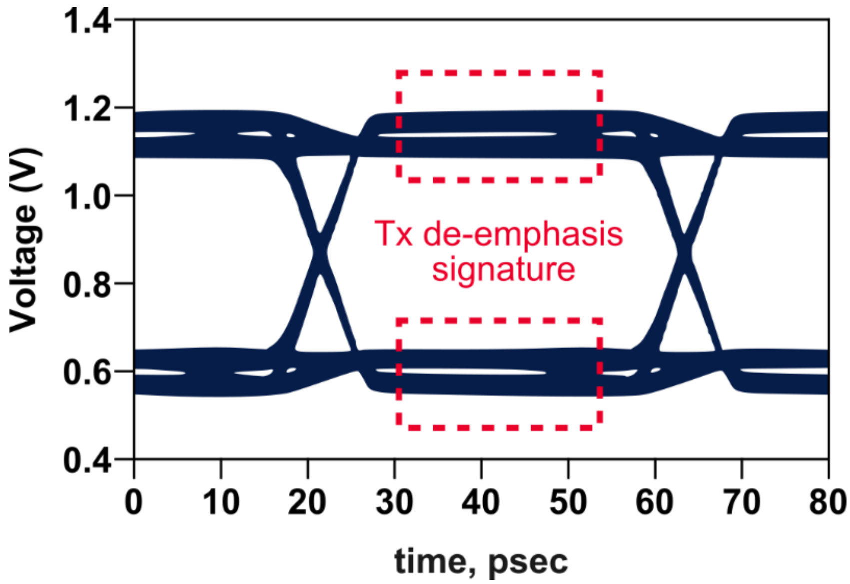

Figure 6. An example of the transmitter eye diagram when the transmitter includes de-emphasis. Equalization can be applied to the transmitter or the receiver to improve the eye-opening.

SI Guidance in the UCIe Standard

Recognizing the upcoming SI challenges in chiplet D2D interconnect designs, researchers and engineers have created standards to guide the industry. One such standard is the Universal Chiplet Interconnect Express (UCIe).

The UCIe standard not only provides physical dimensions for chiplet designs. It also offers electrical layer specifications on the SI of the interconnects. Below are three examples.

VTF loss

One of the unique features of the UCIe standard is the metric, VTF, the voltage transfer function. As shown in

Figure **7** below, the VTF loss metric is a mask that helps determine whether the current interconnect is too lossy. To pass, the VTF loss line of your data line needs to be above the UCIe VTF loss mask.

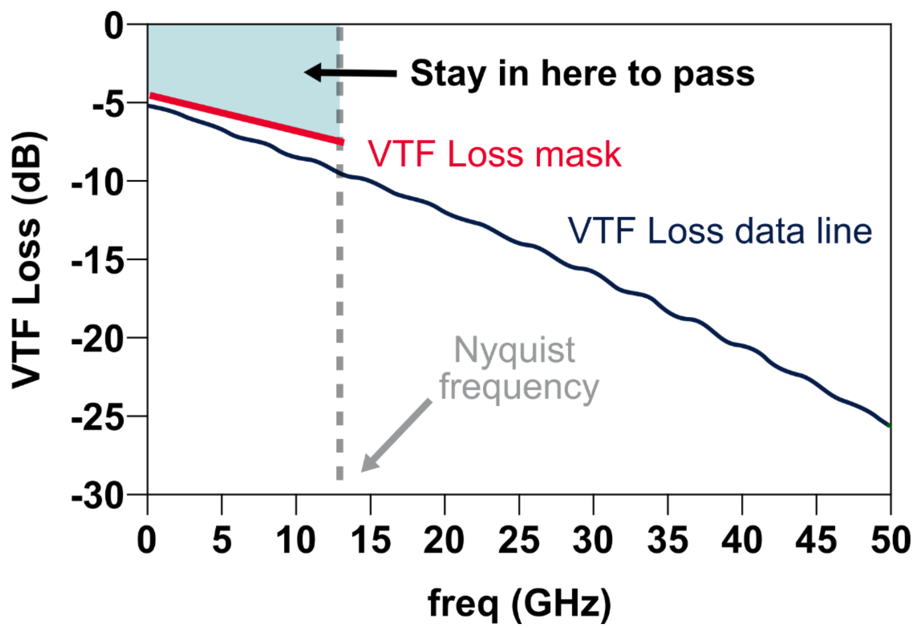

Figure 7. The UCIe standard provides VTF loss metrics for different data rates and packaging types. To pass the VTF loss metric, the VTF loss curve has to stay above the VTF loss mask specified for the given data rate and packaging type.

The main difference between VTF loss and S-parameter insertion loss is that the former includes input and output resistance and capacitance in calculating VTF loss [3].

VTF crosstalk

Similarly, the UCIe standard provides a mask for VTF crosstalk. VTF crosstalk is defined as the power sum of the ratios of the aggressor receiver voltage to the source voltage [3]. Figure 8 below is a data line that fails the VTF crosstalk metric.

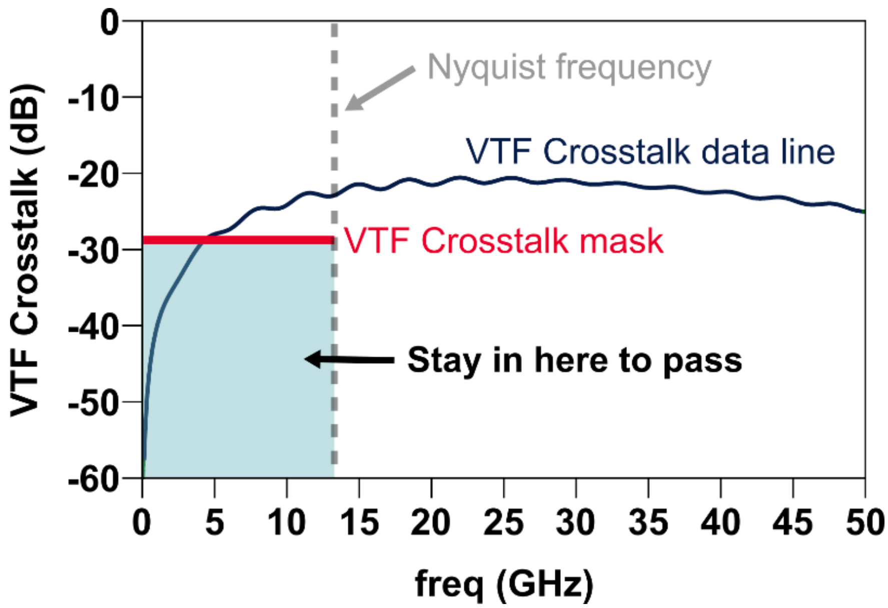

Figure 8. The UCIe standard provides VTF crosstalk metrics for different data rates and packaging types. To pass the VTF crosstalk metric, the VTF crosstalk curve has to stay below the VTF crosstalk mask specified for the given data rate and packaging type.

Eye mask and Equalization

Figure 9 below shows the UCIe standard specified eye masks for 24 GT/s (Giga-Transfer per second). Equalization (EQ) on the transmitter (Tx) is recommended for 16 GT/s.

As the data rate reaches 24 GT/s or 32 GT/s, the UCIe standard requires the implementation of Tx equalization. On the receiver (Rx) side, the standard states that equalization may be implemented at 24 GT/s and 32 GT/s [3].

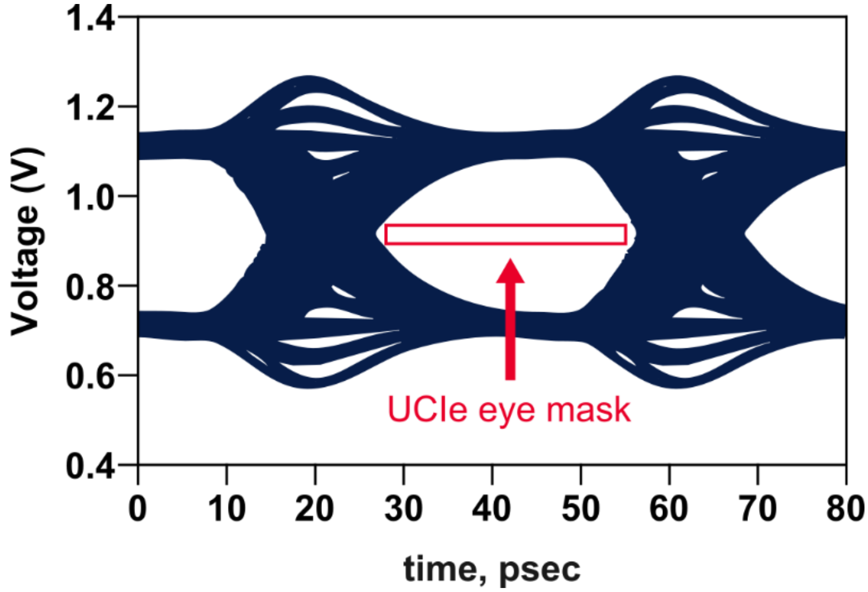

Figure 9. The UCIe standard provides eye masks to evaluate the performance of a given link. Proper Tx and Rx equalization can improve the eye-opening.

Chiplet Analysis with EDA

To address the unique SI challenges in chiplet designs, it is imperative to utilize Electronic Design Automation (EDA) software that offers comprehensive SI analysis capabilities. Key attributes to consider in an EDA solution include:

- **Standards Compliance:** Ensure the software supports chiplet interface standards, facilitating interoperability and compatibility.
- **Complete Link Analysis:** Look for software that offers robust channel link analysis from transmitter to receiver, enabling early identification and resolution of SI issues.
- **Usability and Integration:** Select user-friendly software with a solution that integrates the analysis and verification into your design process.

By selecting the right EDA solution tailored to chiplet design requirements, designers can effectively address SI challenges and unlock the full potential of chiplet-based systems.

Keysight EDA Chiplet PHY Designer

Shown in Figure 10, Chiplet PHY Designer is a part of Keysight EDA Advanced Design System (ADS). It has all the key attributes one seeks when performing chiplet signal integrity analysis.

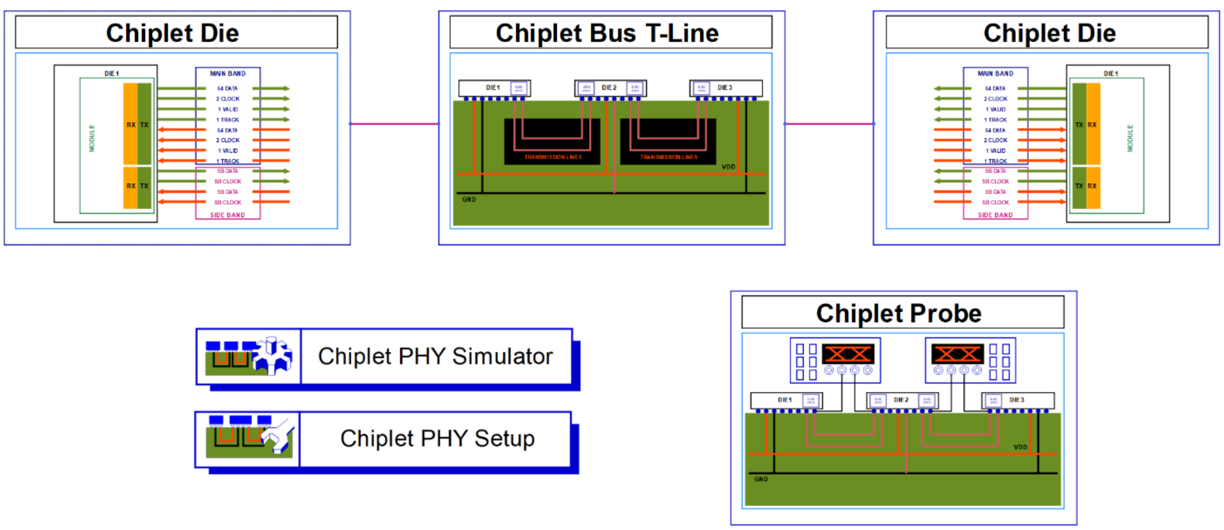

Figure 10. Keysight EDA Chiplet PHY Designer uses the block-based interface to simplify the chiplet die-to-die (D2D) simulation setup. It focuses on different chiplet standards and makes analyzing the full chiplet-to-chiplet link easy.

Standard driven

Figure 11 shows how Chiplet PHY Designer focuses on the chiplet standards. The UCIe standard and its relevant data rate and package type are in a dropdown list. This makes the simulation setup very intuitive.

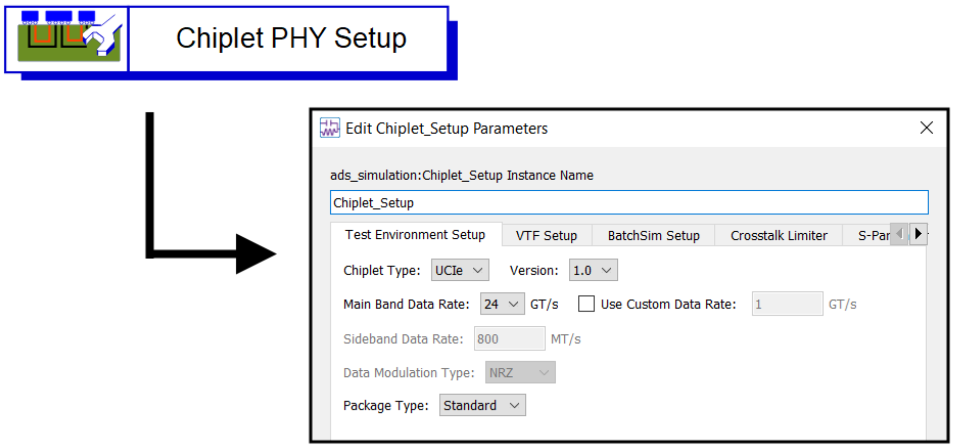

Figure 11. Users can specify different chiplet standards, data rates, and packaging types in the Chiplet PHY Setup component.

Complete link analysis

To best predict the behavior of an entire channel link in simulation, you need to represent the transmitter, receiver, as well as the channel itself.

Chiplet PHY Designer understands the Tx and Rx IBIS-AMI (Input/Output Buffer Information Specification - Algorithmic Modeling Interface) models. Capabilities such as adding equalization, sending the forwarded clock, and setting different termination resistances are a few clicks away. Figure 12 shows an example of using the AMI forwarded clock to sample the analog data signal waveform.

You can model your channel as transmission lines in Chiplet PHY Designer. You could also import any channel S-parameter files from a 3D Electromagnetic (EM) simulation.

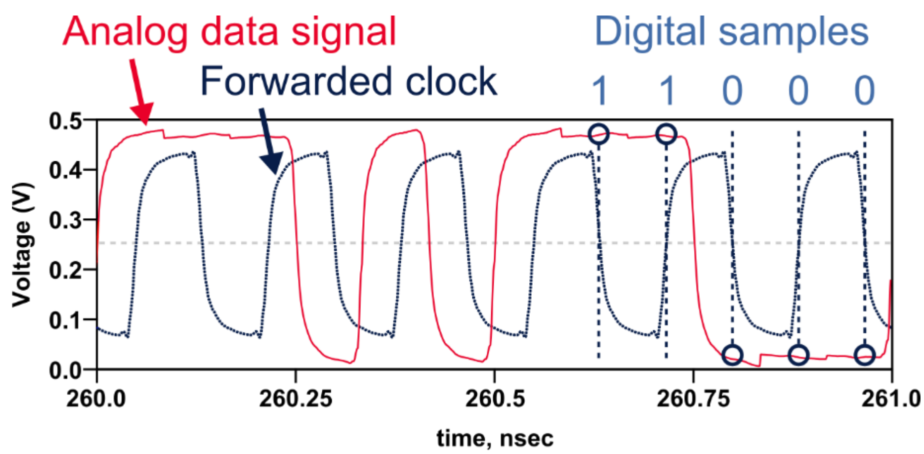

Figure 12. A simulation example of using the forwarded clock in the IBIS-AMI model to examine the analog data signal and the sampled results.

Smart user interface

To reduce the time spent setting up the simulation, Chiplet PHY Designer implemented a smart connection wizard. It uses the signals' names to perform connections. Figure 13 shows the process of connecting 20 or more signal lines with a few clicks.

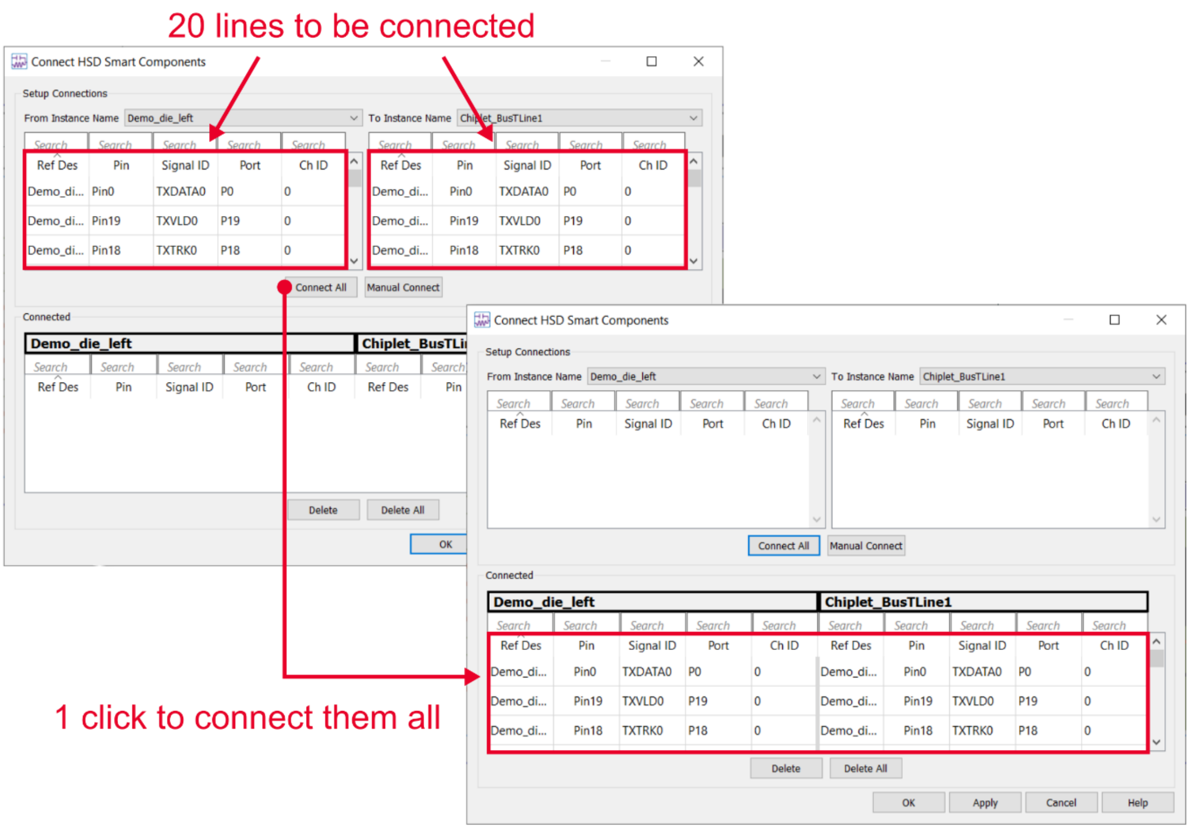

Figure 13. The connection wizard reduces the time spent on making connections. This intelligent feature greatly improves productivity.

Design exploration

If you are deciding between different termination resistances to use, the design exploration feature will help you sweep through the values and generate a report for you, see Figure 14. Design exploration goes beyond sweeping resistance values. It is a wonderful feature that helps you explore the design space while documenting progress.

Chiplet PHY Designer Report

Configuration Details	
Design Name	Chiplet_PHY_Designer_Demo_2024U2_lib:new_design_exploration
Probe Name	Chiplet_Probe
Analysis Mode	StatisticalSim
Technology Type	UCIe
Version	1.0
Data Rate	32 GT/s
Package Type	Standard
Number of Batch Points	5

Ch0_dieRight_RxOutput_RXDATA7

Measurement	Value	Unit	Deviation(%)	Range	Pass or Fail
CustomMaskByShapeMargin Timing Margin P1	2.00521e-12 (0.0641667)	sec (UI)	NA	0.0 to inf (0.0 UI to inf UI)	Pass
CustomMaskByShapeMargin Timing Margin P2	1.64062e-12 (0.0524998)	sec (UI)	NA	0.0 to inf (0.0 UI to inf UI)	Pass
CustomMaskByShapeMargin Timing Margin P3	-1.21094e-12 (-0.0387501)	sec (UI)	NA	0.0 to inf (0.0 UI to inf UI)	Fail
CustomMaskByShapeMargin Timing Margin P4	-6.25e-13 (-0.02)	sec (UI)	NA	0.0 to inf (0.0 UI to inf UI)	Fail
CustomMaskByShapeMargin Min Timing Margin	-1.21094e-12 (-0.0387501)	sec (UI)	NA	0.0 to inf (0.0 UI to inf UI)	Fail
CustomMaskByShapeMargin Voltage Margin P1	0.042	V	NA	0.0 V to inf V	Pass
CustomMaskByShapeMargin Voltage Margin P2	0.034	V	NA	0.0 V to inf V	Pass
CustomMaskByShapeMargin Voltage Margin P3	-0.022	V	NA	0.0 V to inf V	Fail
CustomMaskByShapeMargin Voltage Margin P4	-0.01	V	NA	0.0 V to inf V	Fail
CustomMaskByShapeMargin Min Voltage Margin	-0.022	V	NA	0.0 V to inf V	Fail

Eye Diagrams

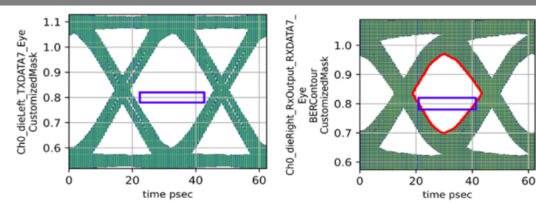

Figure 14. Chiplet PHY Designer helps you explore design space by making it easy to set up sweeps and generate reports.

Explore the Chiplet Frontier with a Good Partner

In conclusion, chiplet design represents a transformative shift in semiconductor manufacturing, offering performance, cost-efficiency, and scalability benefits. However, it also presents unique signal integrity challenges that require detailed analysis to ensure reliable D2D communication.

The Universal Chiplet Interconnect Express (UCIe) standard provides essential SI specifications, addressing key issues such as VTF loss, VTF crosstalk, and eye masks for various data rates. Following the standards is crucial for maintaining robust chiplet communication.

Electronic Design Automation (EDA) tools are vital in identifying potential SI issues. Keysight's Chiplet PHY Designer, part of the Advanced Design System (ADS), exemplifies an effective EDA solution with its standard-driven approach, comprehensive link analysis, and user-friendly interface. This tool simplifies the SI analysis simulation setup, helping designers achieve performance goals.

Resources

Analyze your chiplet interconnect with a free trial license

Download and experience Chiplet PHY Designer

Watch Chiplet PHY Designer in action

References

[1] "Chiplets Are Revolutionizing Semiconductor Manufacturing with More Flexibility and Lower Costs," [Online]. Available: https://sourceability.com/post/chiplets-are-revolutionizing-semiconductor-manufacturing-with-more-flexibility-and-lower-costs

[2] G. Loh, "An Overview of Chiplet Technology for the AMD EPYC™ and Ryzen™ Processor Families," [Online Video], Available: https://youtu.be/wqRAG_5KzBE.

[3] "Universal Chiplet Interconnect Express (UCIe) Specification," July 10, 2023, Revision 1.1, Version 1.0.