APPLICATION NOTE

How to Address USB4 Version 2.0 Transmitter and Receiver Test Challenges

KEYSIGHT

Overview

The Universal Serial Bus Type-C (USB-C) has become a ubiquitous and widely adopted interface in modern electronic devices. The connector supports a smaller form factor, higher data rate, more power capabilities, and flexible connectivity with other protocols. Key USB Type-C focus areas include connecting devices, managing power, and ensuring valid data transmissions.

The USB Type-C connector provides reversibility for ease of use and dynamic power up to 240 W with USB4 protocol. It is backward compatible with USB 2.0, USB 3.2, USB 3.1, and USB4. The alternate mode supports DisplayPort, HDMI, and PCIe® protocols for many new and future devices.

Design and test engineers face several challenges as they integrate USB Type-C into their products while ensuring interoperability and test compliance, especially as the data signaling standards increase in speed, the latest of which is USB4 Version 2.0. As the USB compliance test standards have become more complex, successful testing requires highly accurate and standard-compliant test instruments, software, and fixtures.

This application note covers various key challenges and the solutions for the USB4 Version 2.0 transmitter and receiver tests, including new compliance test requirements to support higher data transmission and additional functionality.

Throughout this document, there are references to various generations of USB4. USB4 Gen 2 and Gen 3 refer to prior generations of USB4 (10 Gb/s and 20 Gb/s per lane, respectively), while USB4 Gen 4 refers to the new USB4 Version 2.0 addition to the standard (40 Gb/s per lane).

What is USB4 Version 2.0?

The USB Implementers Forum (USB-IF) released the USB4 Version 2.0 specification in October 2022. With this latest specification, each link has four bidirectional differential lanes running at 25.6 GBaud PAM3 or 40 Gb/s. In the symmetric mode, each link has two lanes running at 40 Gb/s for an aggregate of 80 Gb/s in each direction. With a new asymmetric mode, the link can transmit three lanes in one direction. The net result is 120 Gb/s in one direction and 40 Gb/s in the other direction in asymmetric mode.

USB Gen 4 uses PAM3 signaling at 25.6 GBaud and 40 Gb/s to increase and double bandwidth, using 11-bit / 17-trit encoding. This slight increase in the fundamental frequency from 10 GHz to 12.8 GHz uses existing USB4 and Thunderbolt 4 cables and connectors. For physical layer (PHY) electrical validation engineers, the four differential pairs run at 25.6 GBaud, PAM3, and 40 Gb/s. Table 1 shows a list of changes between USB4 Version 2.0 (Gen 4) and USB4 (Gen 2 and 3).

Specification	USB4	USB4 Version 2.0
Aggregated data rate	40 Gb/s	80 Gb/s
Number of lanes	2 Tx, 2 Rx	2 Tx, 2 Rx
Data rate per lane	20 Gb/s	40 Gb/s
Baud rate	20 GBaud	25.6 GBaud
Signaling	NRZ	PAM3
Asymmetric mode	No	Yes

Table 1. USB4 and USB4 Version 2.0 specification differences

These combined changes to the USB standard create additional challenging USB transmitter and receiver conformance test criteria. Understanding the USB Type-C and USB4 Version 2.0 transmitter and receiver test challenges helps to ensure successful USB Type-C integration and test for devices.

USB4 Version 2.0 Simulation

The cost of revising designs and manufacturing silicon is high and can add significant delays for developers trying to be first-to-market. A key component of reducing these risks is to perform rigorous end-to-end simulation of the entire USB 80 Gb/s link.

To enable early design-stage simulations and extensive system-level post-layout analysis, simulation solutions for USB4 Version 2.0 incorporate Input/output Buffer Information Specification algorithmic modeling interface (IBIS-AMI) model makers to facilitate the development of models for USB devices. Designers can use IBIS-AMI models in channel simulations to predict and simulate the BER, eye metrics, and other design parameters.

With the USB4 Version 2.0 standard, signal frequency, and speeds increase in printed circuit boards (PCBs), so signal and power integrity are critical considerations for any design. Losses associated with transmission line effects cause failures in USB Gen 4 devices. It is crucial to model traces, vias, and interconnects to simulate the board accurately. This process improves high-speed link performance in PCB designs with integrated circuit design and electromagnetic simulators customized for power and signal integrity analysis.

Read more about USB simulation solutions in How to Correlate USB Type-C Simulation and Measurement.

USB4 Version 2.0 Transmitter Test Challenges

Validating USB4 products is already substantially more complex than USB 3.2. USB4 Version 2.0 takes the complexity to a higher level with additional test requirements and signal integrity challenges associated with faster, multilevel signaling that increases the product validation time.

Each transmitter compliance test presents challenges for USB4 Version 2.0 or USB4 Gen 4 PHY designs. Changes to the test specification for USB4 Gen 4 PHY include the following:

- Different test point definitions.
- New vertical margin measurements of the PAM3 signal.
- Higher number of equalization presets.
- New retimer measurements.

Test points

To ensure precise transmitter characterization, developers need to understand the key test points (TPs). The standard defines the output of the compliance test fixture at TP2. Figure 1 illustrates where all transmitter measurements take place. In contrast to USB4 Gen 2 and 3, taking measurements at TP3 for USB4 Gen 4 is no longer a requirement. However, developers should always perform a captive / tethered cable device measurement at TP3 because the only accessible measurement point is at TP3.

Test point	Description	Comments
TP1	Transmitter IC output	Not used for Gen 4 electrical testing
TP2	Transmitter port connector output	Defined at the output of a compliance plug fixture
TP3	Receiver port connector output	Defined at the receptacle side of the connector. All measurements at this point shall be done while applying the reference equalization function
TP3′	Receiver port connector input	Defined at the output of a compliance plug fixture
TP4	Receiver IC input	Not used for Gen 4 electrical testing

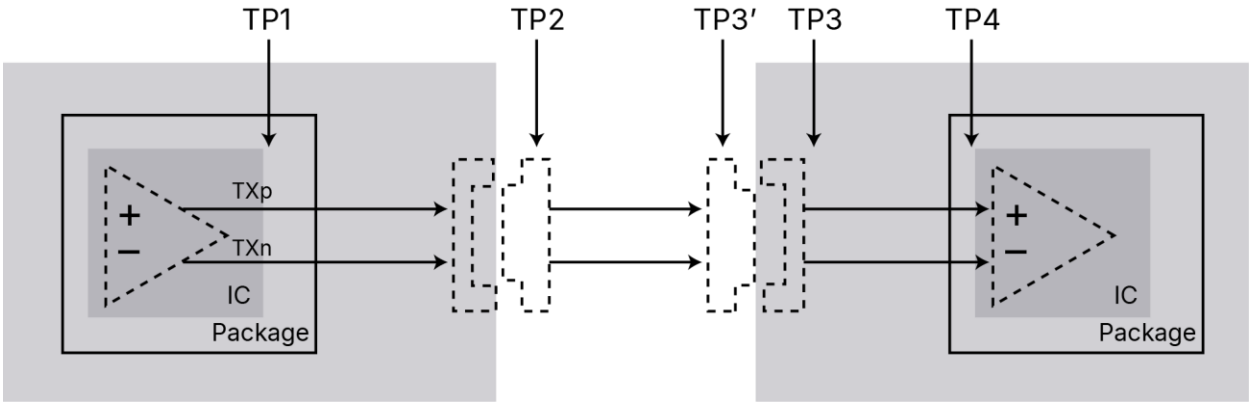

Figure 1. USB4 Gen 4 compliance test point definitions

Vertical noise margin

The new standard carries over traditional jitter and timing measurements from USB4 Gen 2 and 3, performed on the PAM3 signal. Figure 2 illustrates that the most significant challenge with Gen 4 is measuring the vertical signal margin.

There are several new vertical measurements introduced with Gen 4 that ensure acceptable bit error rate (BER) performance:

- The level_mismatch compares the difference in the eye opening between the *top* and *bottom* PAM3 eye.
- The signal and noise distortion ratio (SNDR) is another key vertical margin parameter and uses linear fit pulse response (LFPR) sigma *n* and sigma *e*.
- The integrated return loss (IRL) considers the signal quality at the transmitter coupled with the insertion loss (IL) of the channel for another important vertical margin parameter.

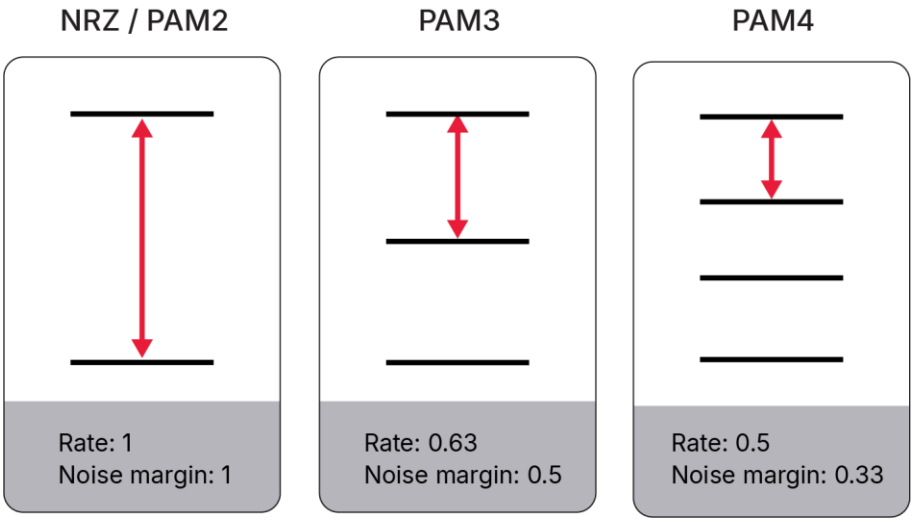

Figure 2. PAM3 has a reduced vertical noise margin compared to non-return-to-zero (NRZ) signals

Equalization presets

USB Gen 2 and 3 had 16 transmitter equalization presets. To accommodate for the increased losses, Gen 4 has 42 presets. Like prior generations, all 42 presets require a sweep to characterize each individually to determine the optimal preset for minimum data-dependent jitter (DDJ).

Retimer measurements

If a USB 80 Gb/s product is larger than a USB stick, it will require retimers. This method requires a clock-switch measurement like the frequency variation training measurement. As the USB-IF updates the standard, you can expect more information about retimer measurements.

USB4 Version 2.0 Receiver Testing Challenges

Receiver-stressed signal calibration is cumbersome because it requires the fine adjustment of several signal impairments. In the case of USB4 Gen 2 and Gen 3, developers must tune the launch voltage, random jitter, sinusoidal jitter, and common mode interference to obtain the right stress level defined in terms of total jitter and eye diagram opening. In the case of USB4 Gen 4, developers adjust the same impairments, as well as differential-mode interference and near-end crosstalk, to obtain the right stress level defined in terms of SNDR and jitter.

A high-bandwidth oscilloscope with the USB-IF SigTest utility measures the stressed signal from the pattern generator. The USB-IF SigTest is a command-line tool that takes a digitized waveform and numerous configuration parameters as input to perform clock recovery and equalization (if applicable) and returns noise, jitter, and other measurements mentioned above.

Like USB4 Gen 2 and 3, Gen 4 has similar stress cocktail components such as launch voltage, alternating current common mode (ACCM), periodic jitter (PJ), random jitter (RJ), and loss channel. Gen 4 receiver testing introduces new vertical stress components like SNDR, level mismatch, differential mode sinusoidal interference (DMSI), and common mode sinusoidal interference (CMSI).

After calibrating the stressed eye, the receiver is ready for testing. The receiver test process encompasses two phases: link training and error counting. During the link training phase, the device under test (DUT) requests various equalization settings from the pattern generator. It adjusts its receiver equalization to improve the quality of the received signal.

During the error count phase, the receiver error counter performs a bit error ratio (BER) test (in the case of Gen 2 and Gen 3) and a trit error rate (TER) test in the case of Gen 4. The USB4 sideband channel communicates with the DUT via the USB-IF's USB4 electrical test tool (ETT) and the USB4 microcontroller.

Like Gen 2 and 3, there are two primary test cases:

- Short channel for low-loss products or link partners connected with active cable.
- Long channel for link partners connected with a passive cable.

Gen 4 added a third test case for link partners connected to a linear redriver (LRD) cable. Like Gen 4 transmitter testing, there is also a special test case for tethered / captive devices. The compliance test specification (CTS) draft version requires adding aggressors for receiver testing.

Like Gen 2 and 3, sideband (SB) testing is a requirement to ensure proper link negotiation. The USB-IF plans to introduce new transmitter and receiver low frequency periodic signaling (LFPS) testing requirements with Gen 4. Gen 4 added the asymmetric operation mode that also requires specialized testing.

USB4 Version 2.0 Transmitter and Receiver Return Loss

USB4 Gen 2 and 3 introduced new differential and common mode return loss requirements for transmitter and receiver testing, which carries over into Gen 4. Return loss — the ratio of reflective power to incident power — is the direct measure of the impedance match of a transmission line. Meeting the test limit requirement is critical to meet compliance certification and ensure product performance and interoperability.

In USB4 Version 2.0, the USB-IF introduced the IRL measurement. Figure 3 illustrates that the differential return loss requirement remains one of the informative items for compliance certification. The increased bit rates to 80 Gb/s to support USB4 Version 2.0 protocol introduce additional signal integrity challenges and require a more stringent integrated (summed) return loss test corresponding to the integrated power spectral density of the incidental / reflective behaviors over the baseline baud rate frequency range.

You can extract the transmitter IRL as follows:

$$IRL = 20 \times \log_{10}\left(\sqrt{\frac{\int_0^{20\,GHz} |V_{in}(f)|^2 \cdot |S_{dd22}(f)|^2 df}{\int_0^{20\,GHz} |V_{in}(f)|^2 df}}\right)$$

where:

- Sdd22(f) is the return loss of the transmitter at TP2, referenced to a single-ended load impedance of 42.5 Ω.
- Vin(f) is the spectrum of the ideal PAM signal with a 20% slew rate, defined as $Vin(f)$ = sin ($\pi \cdot f \cdot Tr$) / $\pi \cdot f \cdot Tr$ * sin ($\pi \cdot f \cdot Tb$) / $\pi \cdot f \cdot Tb$, with Tb = 39.0625 ps and Tr = 0.2·Tb.

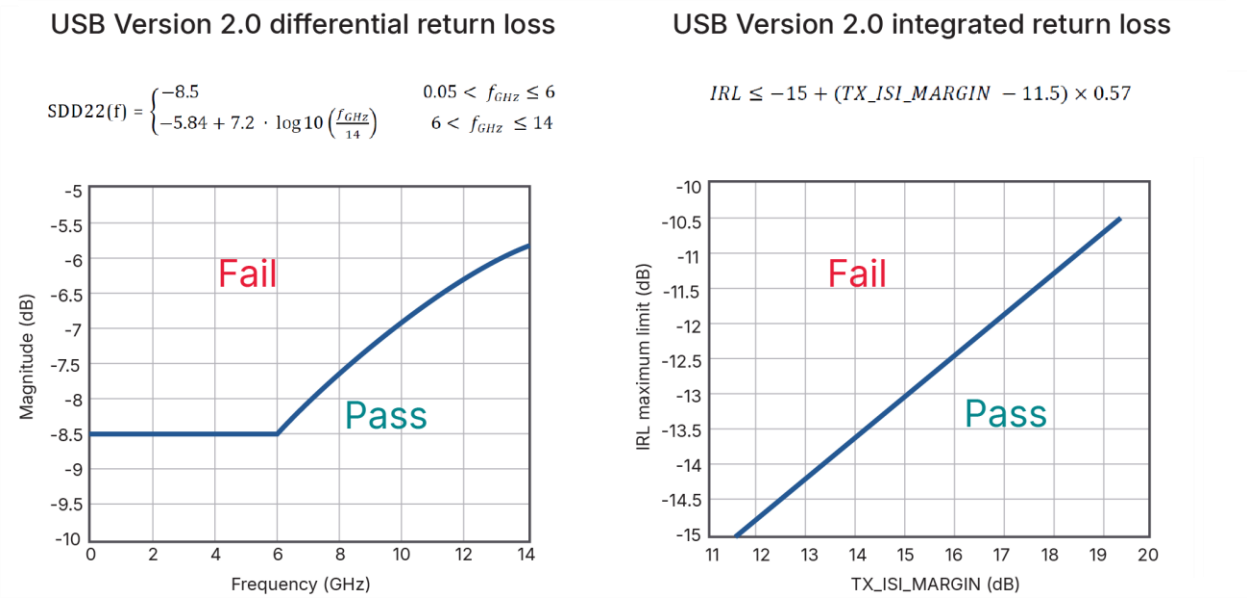

Figure 3. USB4 Version 2.0 transmitter and receiver return loss test limit requirement

Figure 4 shows the transmitter and receiver differential return loss (Sdd22) and IRL setup. A vector network analyzer (VNA) measures an S-parameter touchstone file (S2P), while the transmitter / receiver DUT is in active mode with PRBS7 pattern driving by a USB4 test microcontroller and ETT tool. The SigTest tool analyzes the measured S-parameter for delivering test results.

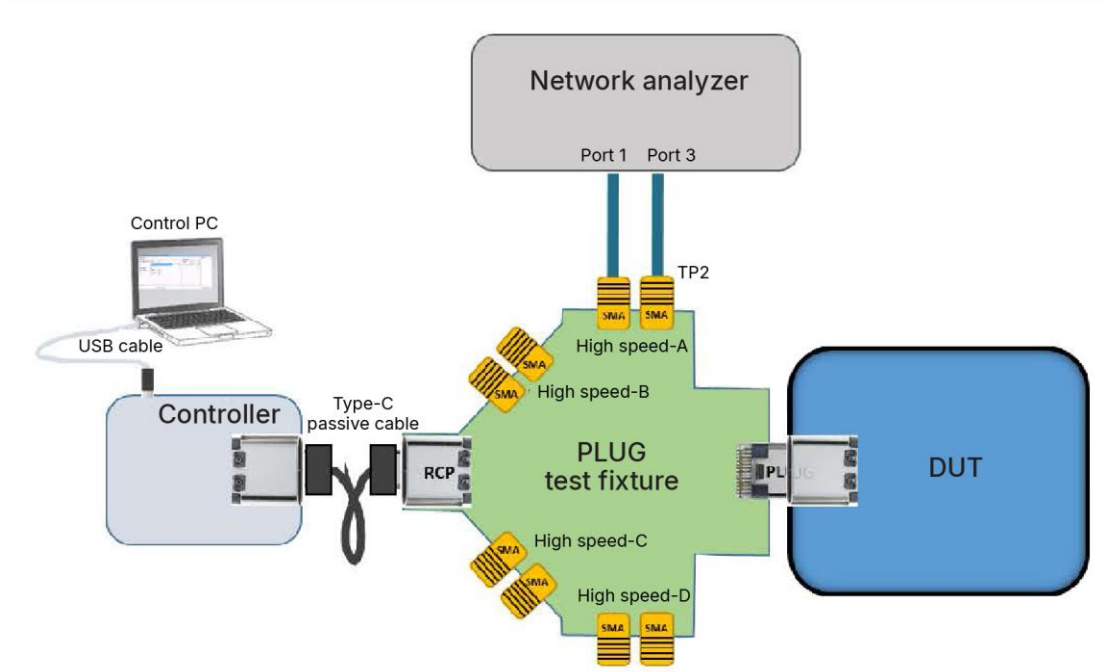

Figure 4. USB4 Version 2.0 transmitter and receiver return loss proposed test setup

The transmitter IRL maximum limit is a function of the measured transmitter intersymbol interference (ISI) margin (transmitter_ISI_margin) which corresponds to the transmitter signal-to-residual ISI ratio. The USB SigTest tool must compile a waveform file (.bin) of ui_jitter_vertical for the transmitter's timing and voltage measurement test to verify the verdict of the transmitter IRL, as shown in Figure 5.

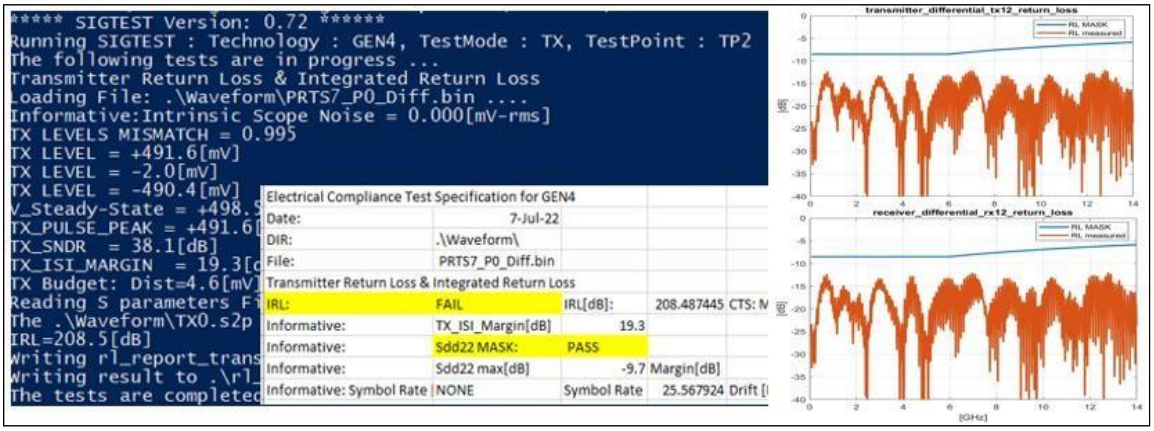

Figure 5. Sample of the test result from USB4 SigTest compilation

In the transmitter and receiver return loss test, it may be possible in some cases for the transmitter or receiver signaling of the DUT to introduce error into the measurement. For example, the DUT is not transmitting the proper pattern, or the system forces the DUT into the incorrect mode. It can produce erroneous measurement results, which could lead to false failures. Developers should take care to minimize all sources of error.

Developers should warm up the VNA used for the measurement and calibrate it with an electronic calibration module (eCal) prior to the measurement. The VNA's setup should follow proposed CTS requirements with Port 1 and Port 3 connected to the DUT with a sweep frequency range from 50 MHz to 20 GHz and intermediate frequency bandwidth (IFBW) of at least 1,600 points to minimize the trace noise.

New Test Requirements for USB4 Gen 3 and Gen 4 Cables

Compared to the previous USB 3.2 Type-C CTS, USB4 Type-C CTS is much more complex. The increased bit rates to 40 Gbps / 80 Gbps to support USB4 and USB4 Version 2.0 protocols introduce additional signal integrity challenges and require more stringent integrated test parameters corresponding to the incidental/reflective behaviors over a frequency range.

The aim of the new test group — test group B-8 and test group A-8 — requirements are for the integrated S-parameters except for insertion loss and differential-to-common-mode conversion. These test groups mitigate the potential rejection of a functioning cable assembly that may fail the traditional S-parameters specification at a few frequencies. In the case of integrated return loss, it now manages the reflection between the cable assembly and the rest of the system (host and device).

Read more about Type-C cable and interconnect testing in How to Ensure Interoperability and Compliance of USB Type-C Cables and Connectors.

Transmitter Test Solutions

Choosing the right measurement solution for USB compliance testing is crucial to ensure it meets the USB-IF compliance test specifications and the highest interoperability performance. Figure 6 illustrates the Keysight D9350USBC transmitter test application for the USB4 Version 2.0 specification for USB4 Version 2.0 transmitter compliance testing. This solution provides a fast and easy way to test, debug, and characterize your USB 80 Gbps products.

The tests performed by the D9350USBC software use the USB-IF requirement — USB4 Version 2.0 CTS and SigTest. The test application offers a user-friendly setup wizard and a comprehensive report. In addition to the compliance test software, the measurements require D9320ASIA advanced signal integrity software for de-embedding PAM3 channels.

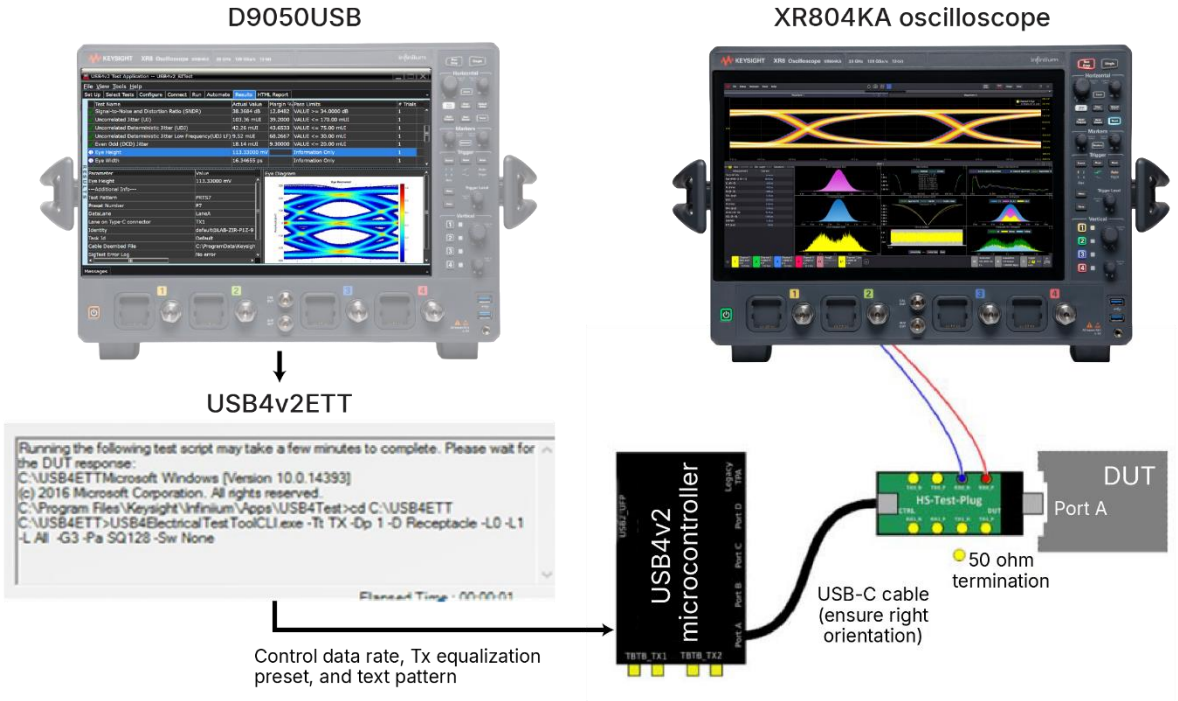

Figure 6. Keysight test setup for USB4 Version 2.0 transmitter compliance testing

The automated test software runs on the Keysight XR8 oscilloscope, which supports transmitter and receiver testing measurements. USB4 Version 2.0 compliance testing requires an oscilloscope with at least 25 GHz of bandwidth and two channels minimum. Silicon developers require an oscilloscope supporting 50 GHz bandwidth for characterization and testing.

Receiver Test Solutions

The Keysight N5991U42A receiver compliance test automation software simplifies calibration and receiver testing for USB devices. The software walks developers through the receiver testing setup and automates testing for the entire USB4 Version 2.0 compliance test specification. Figure 7 shows that the all-in-one solution increases test speed, reduces test costs, and ensures greater thoroughness and repeatability than manual tests for USB prototypes, development boards, or chipsets.

Figures 7 and 8 show the N5991U42A communicating with the DUT directly to fully automate calibration and testing. This software also supports additional testing beyond the compliance test suite, including the jitter tolerance characterization and sensitivity tests. This solution ensures that the USB device interoperates with any other product on the market.

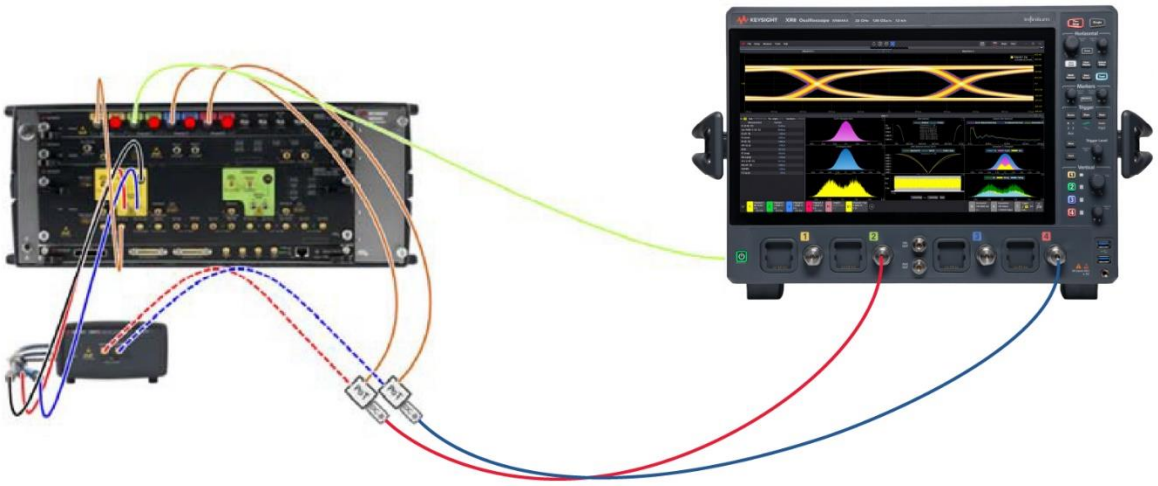

Figure 7. N5991U42A test solution for USB4 Version 2.0 receiver calibration

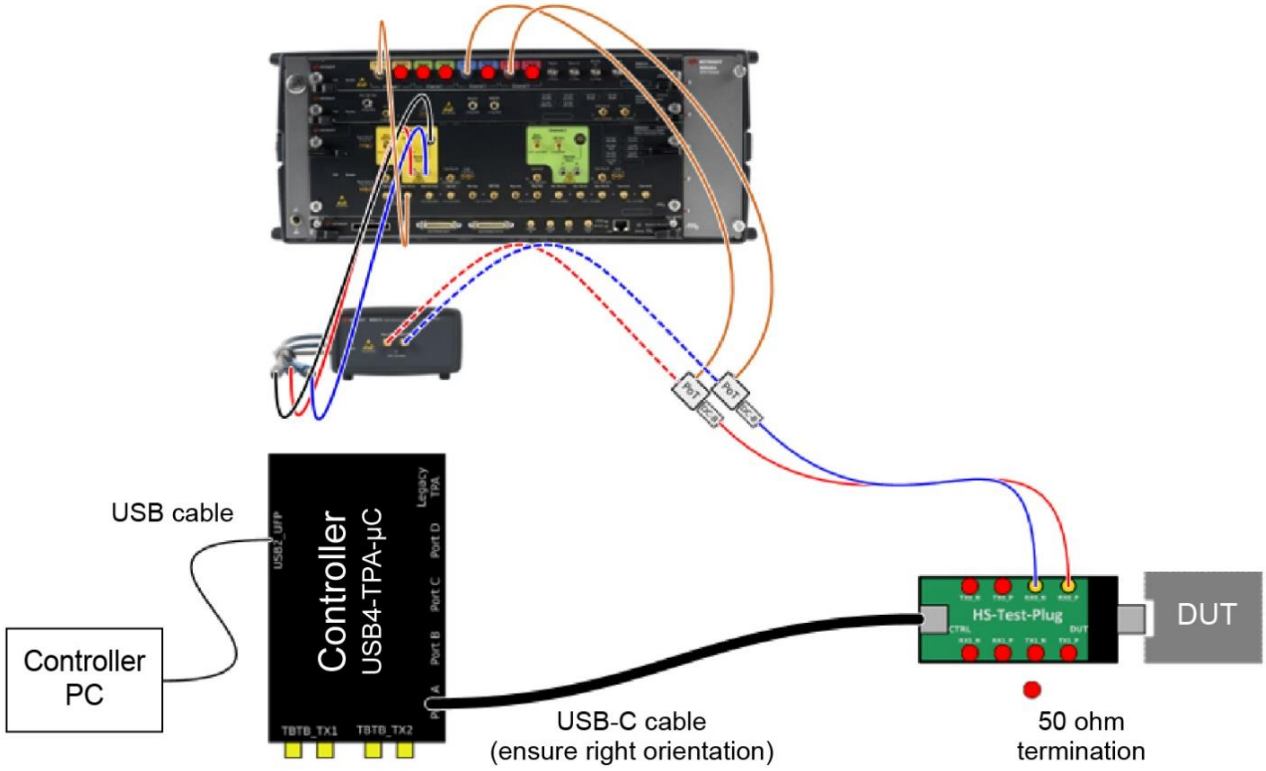

Figure 8. Keysight test solution for USB4 Version 2.0 receiver compliance testing

The compliance software runs with the Keysight M8040A high-performance 64 Gbaud BERT, which has everything you need built into the equipment (de-emphasis, pattern capabilities, continuous-time linear equalization (CTLE), decision feedback equalization (DFE), the capability to create the various pattern structures and resequencing). Receiver calibration requires a 25 GHz bandwidth oscilloscope with D9320ASIA advanced signal integrity software.

Summary

The physical layer (PHY) silicon intellectual property (IP) development kits, simulation solutions, and test and measurement solutions reviewed in this application note are the foundational blocks required for silicon and system integrators to design compliant USB4 Version 2.0 products that meet strict interoperability requirements in the vast Type-C ecosystem.

The USB4 Version 2.0 specifications introduce many new USB transmitter and receiver test challenges. USB Gen 2 / 3 at 10 / 20 Gb/s NRZ continues to be challenging to implement. Even more complicated is USB Gen 4 at 25.6 GBaud PAM3, 40 Gb/s 11-bit / 7-trit encoding, coupled with asymmetric mode, crosstalk, and the same loss channel.

The smaller vertical noise margin and its associated measurements, an increase in equalization presets, and retimer measurements are critical aspects of transmitter testing. Receiver testing is more complex than USB4 Gen 2 and 3 due to new differential-mode interference, near-end crosstalk adjustments during calibration, and new trit error rate (TER) measurements during the error counting phase.

The Keysight USB testing solution — software, instruments, and fixtures — is ready for complete testing of the standards converging on this universal interface. Whether you focus on design or validation, our solution accelerates the debugging process to help you with characterization and USB4 Version 2.0 compliance.