Jitter & Crosstalk Analyses/ Compliance Testing

Keysight	***2025.05.14***
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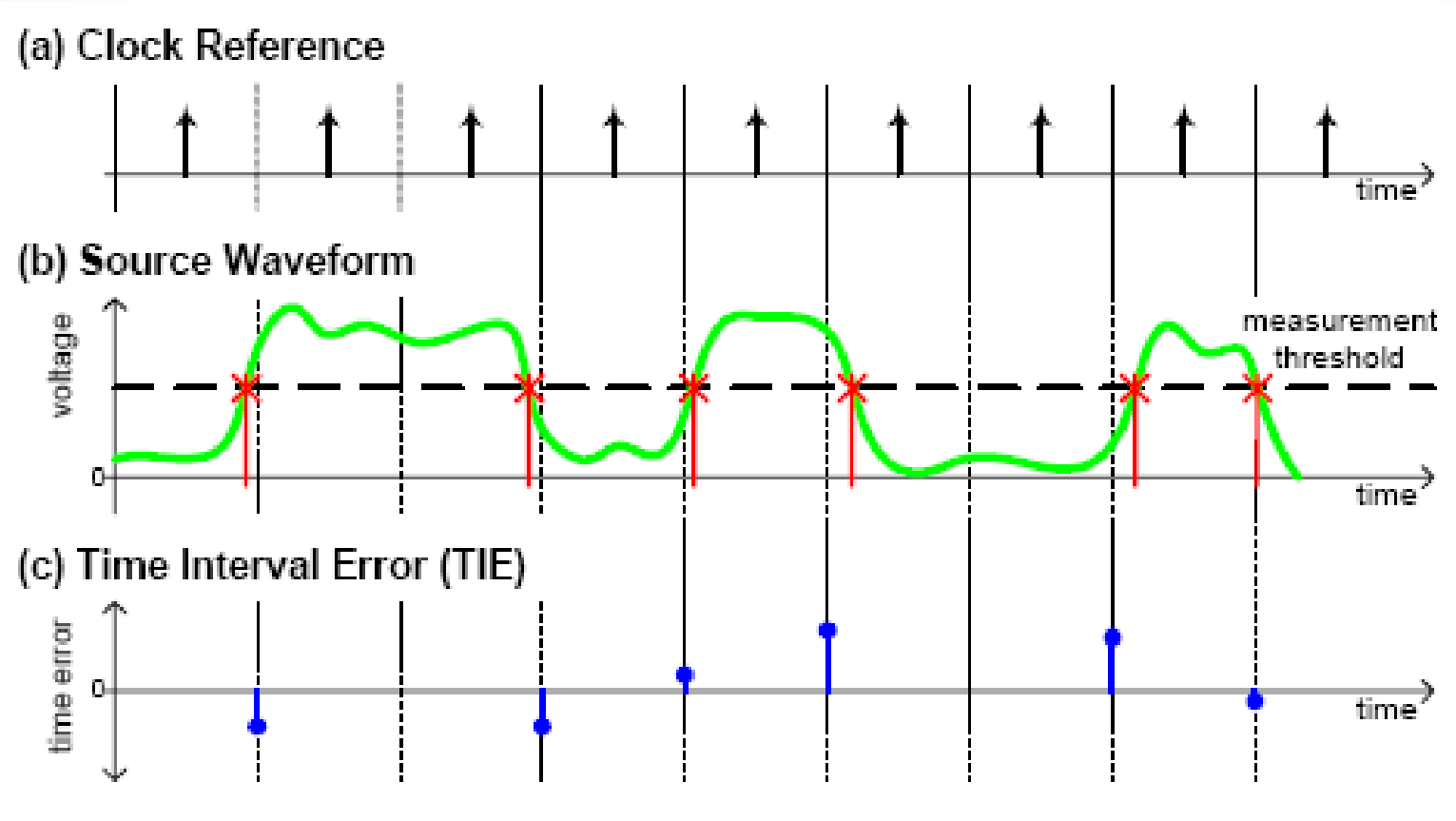
Agenda

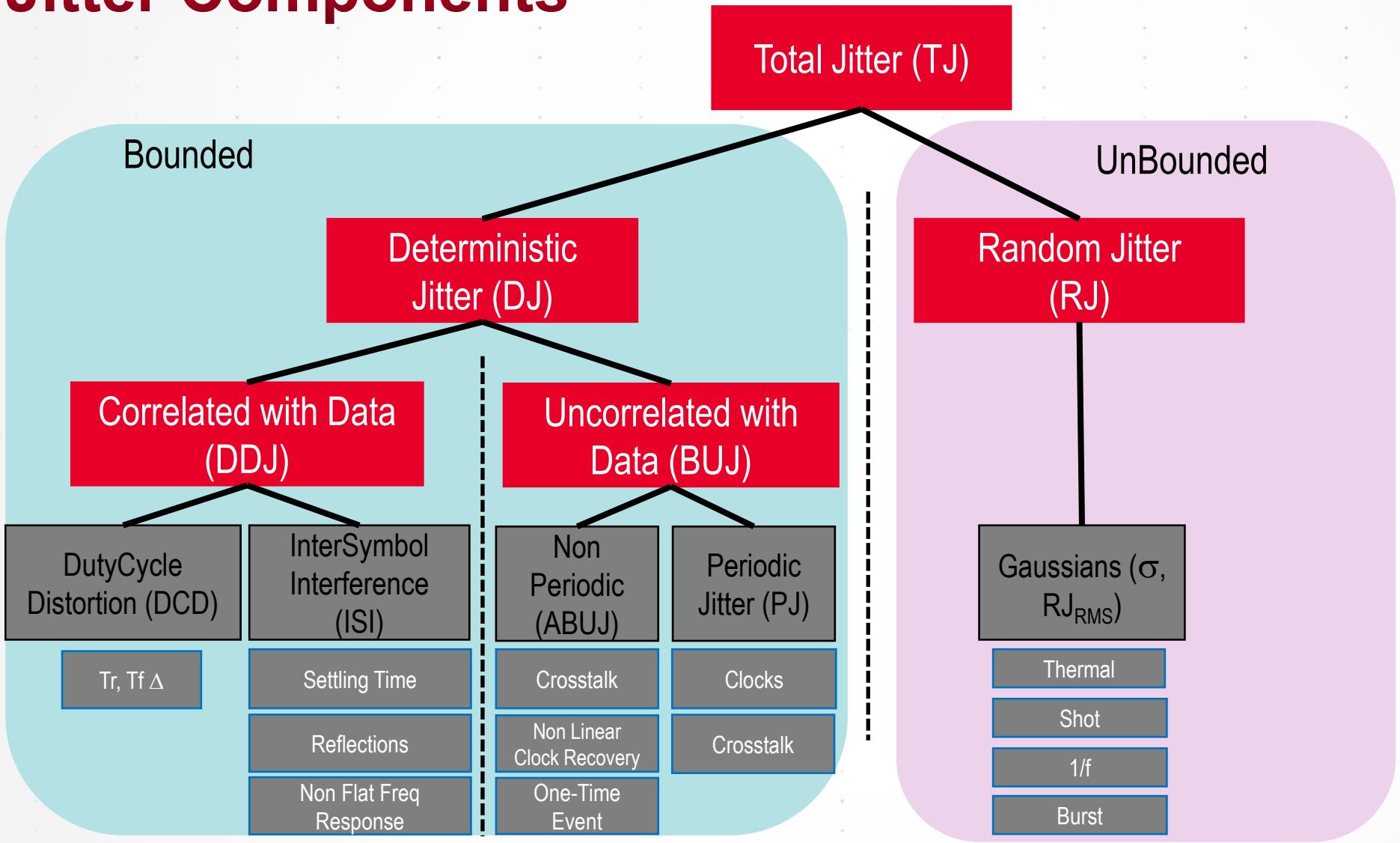
- Review of Jitter Decomposition
- Assumptions and Limitations
- Other Tools to Consider for Jitter Analysis
- Crosstalk Analyses and Removal
- Basics of Compliance Testing

Jitter and Time Interval Error (TIE)



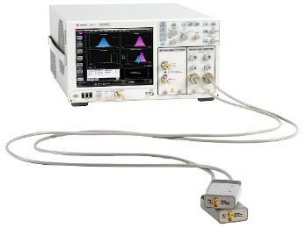
On an oscilloscope we monitor the waveform transitions and note the jitter at each transition point. This is called the Time Interval Error (TIE) record.

Jitter Components



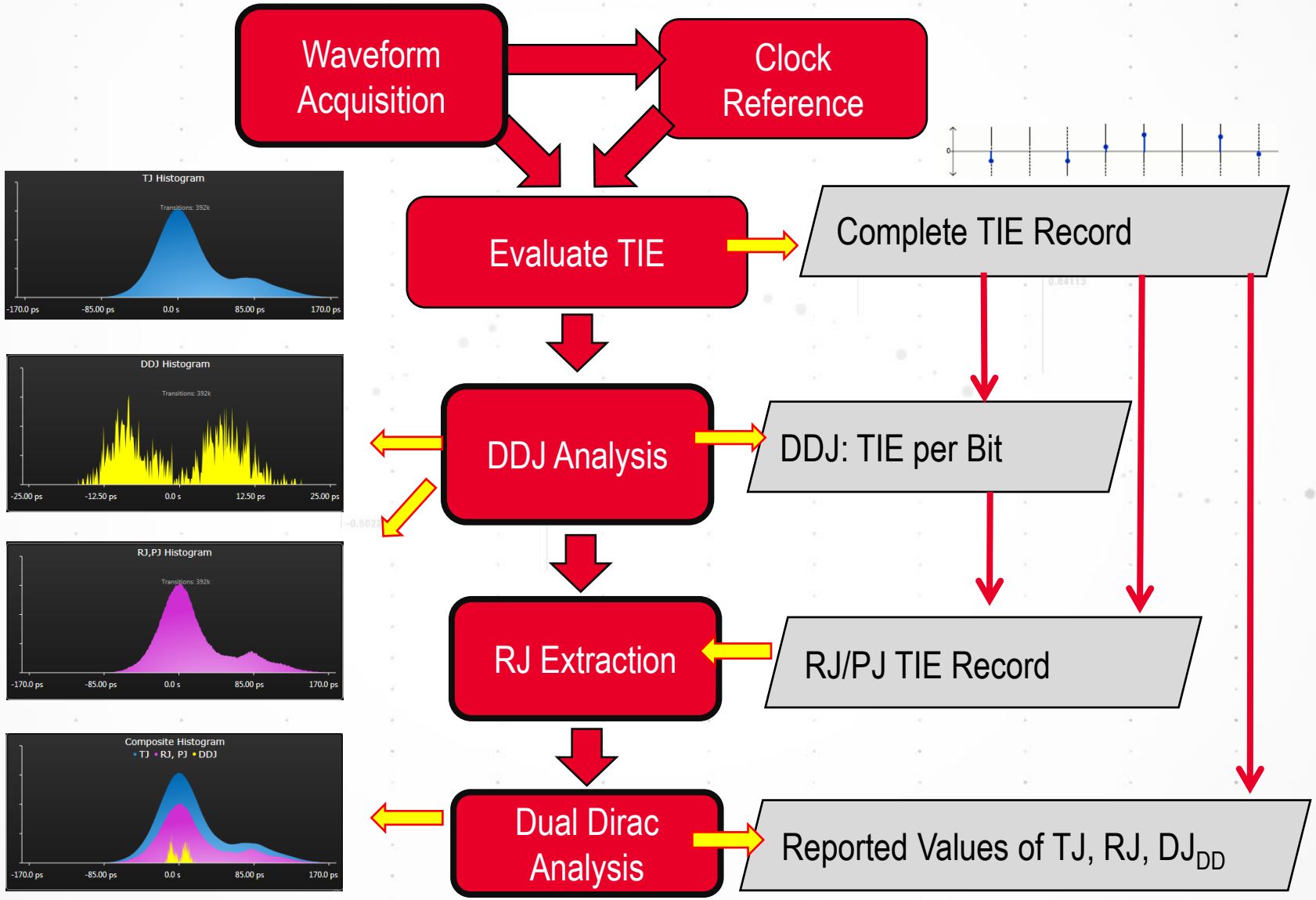
Acronyms:
DDJ: Data Dependent Jitter
BUJ: Bounded Uncorrelated Jitter
ABUJ: Aperiodic Bounded Uncorrected Jitter

Instruments for Jitter Analysis



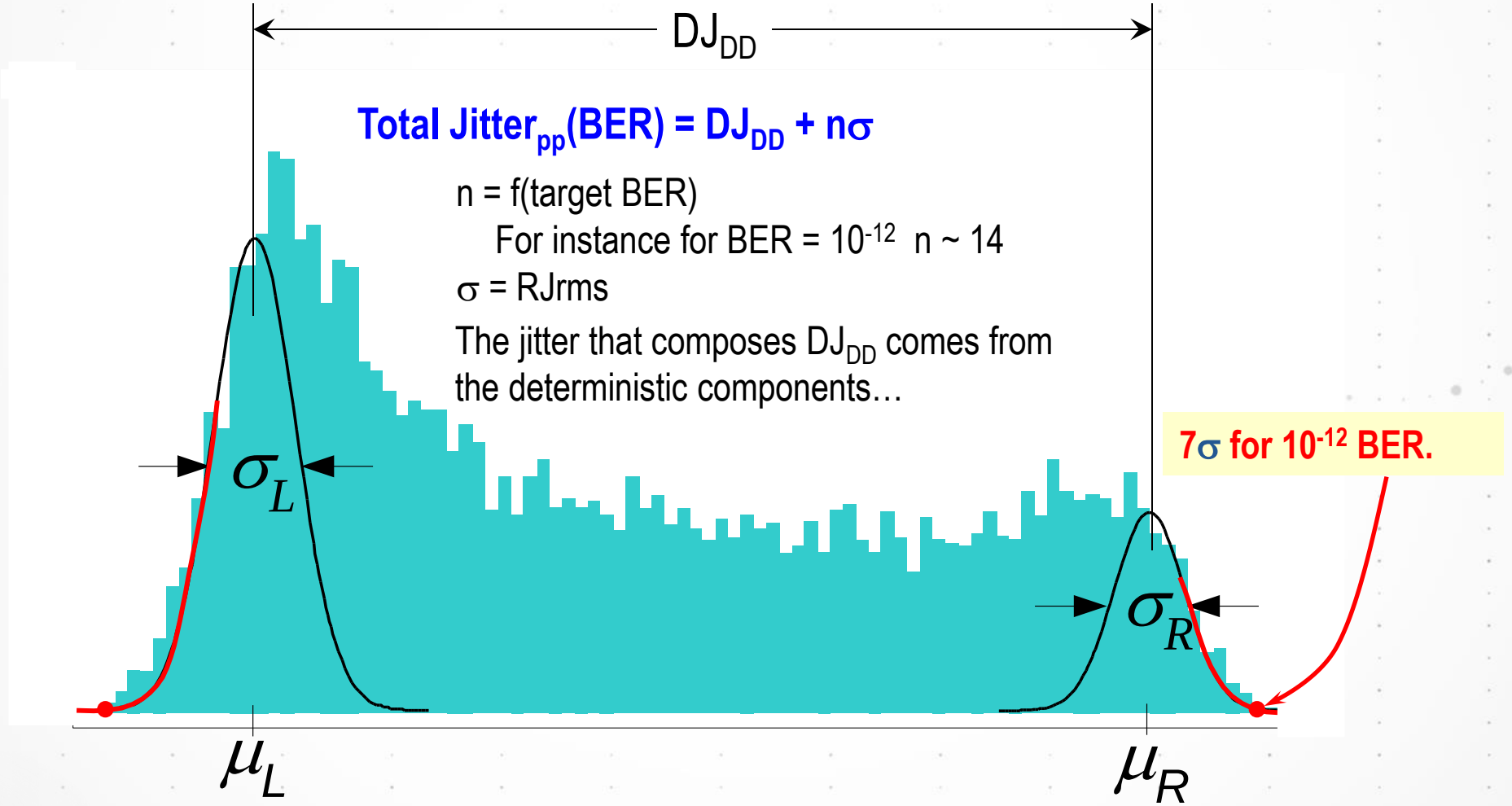
Descriptions	Real-Time Scope	Sampling Scope	Bit Error Ratio Tester (BERT)
Measurement	Estimates jitter	Estimates jitter	Measures jitter
Analysis mode	Based on Dual-Dirac Model	Based on Dual-Dirac Model	Accumulate and compare 3 times the BER level bits for 95% confidence level E.g. $3x10^{12}$ bits are received without error to meet the 10^{-12} BER target
Clock reference	Software clock recovery and accepts explicit clock	Hardware clock recovery	Hardware clock recovery
Speed	Fast (Seconds)	Fast (Seconds)	Slow (Minutes or Hours) - depends on time to accumulate the bits
Report jitter components	Yes	Yes	No

Jitter Decomposition Overview

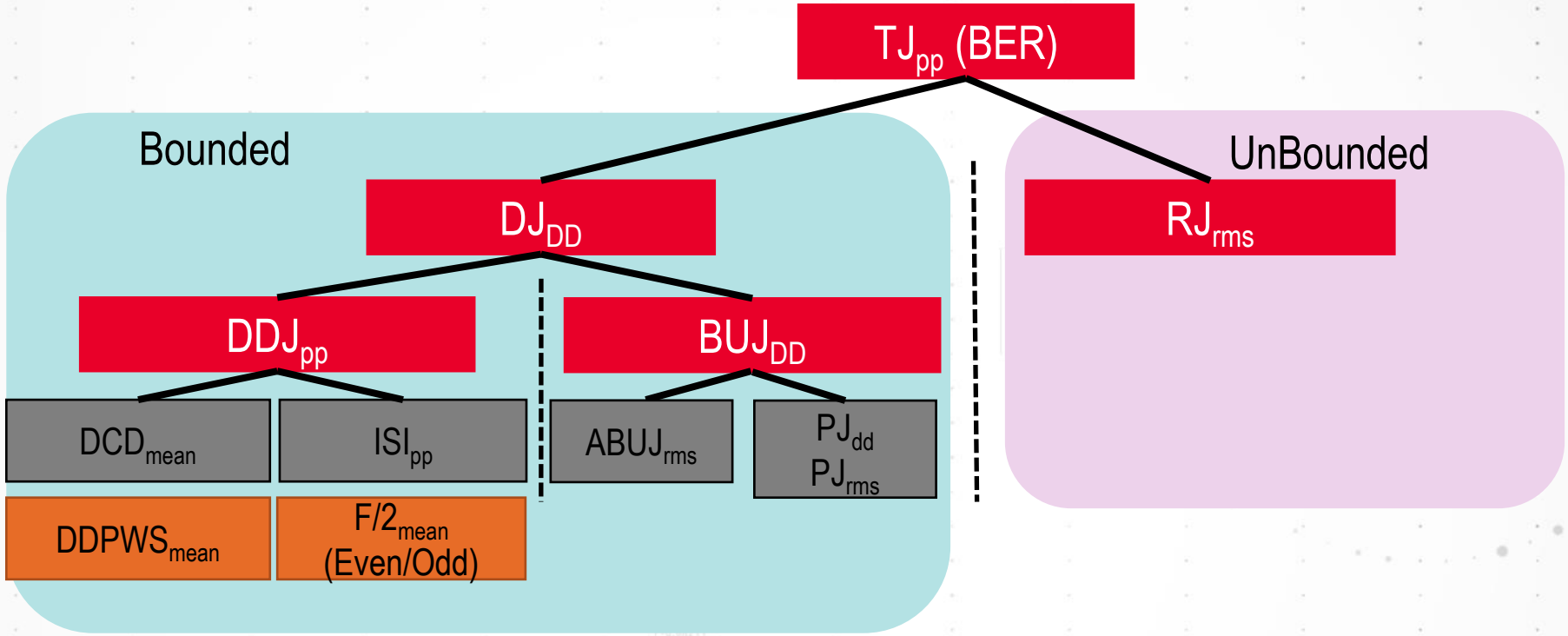


Jitter Decomposition with Dual Dirac Assumption

FIT THE **RJ GAUSSIAN CURVE TO BOTH** TAILS OF THE TIE HISTOGRAM OR JITTER PROBABILITY DENSITY FUNCTION (PDF)



Jitter Components Reported by Scope and the Caveats

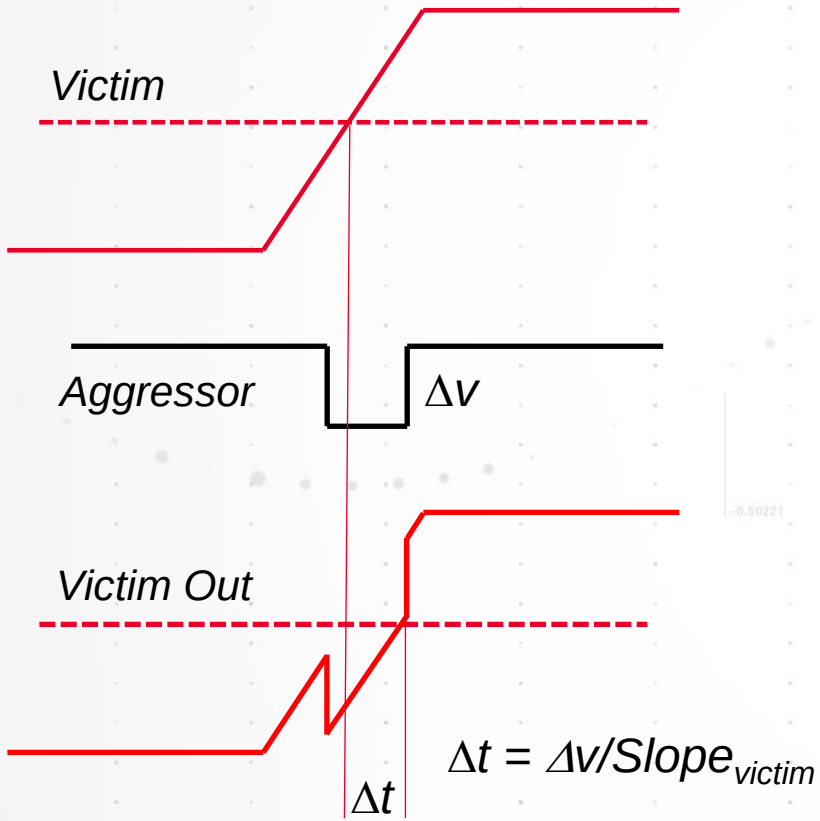


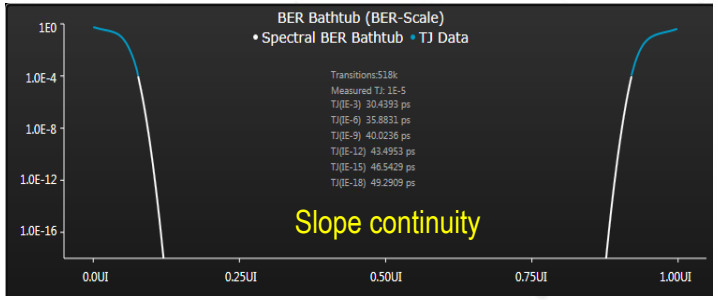
Caveats of jitter decomposition:

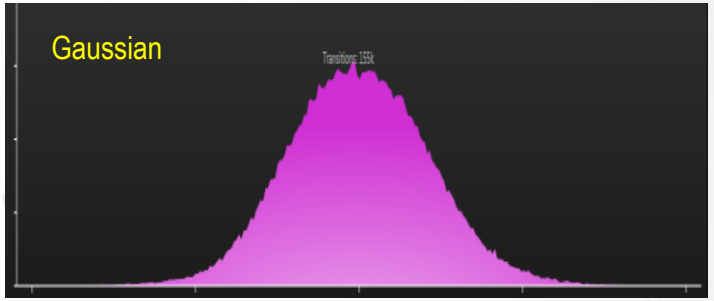
1. Jitter decomposition does not follow a linear bottom-up flow.
2. Algorithm is based on Dual-Dirac model and is an approximation, not the exact value.
3. Each jitter component may have a different unit value (rms, dual-dirac (dd), peak-to-peak (pp), mean, etc.)
4. Not every component has a result. Some are convolved with other components and not separable.
   - E.g. DJ_{pp}, PJ_{pp}, $ABUJ_{dd}$ and $ABUJ_{pp}$ (crosstalk) are not separable and reported.
5. Other jitter components can be calculated separately from the jitter decomposition algorithm (in orange).

ABUJ: Crosstalk or Ground Bounce

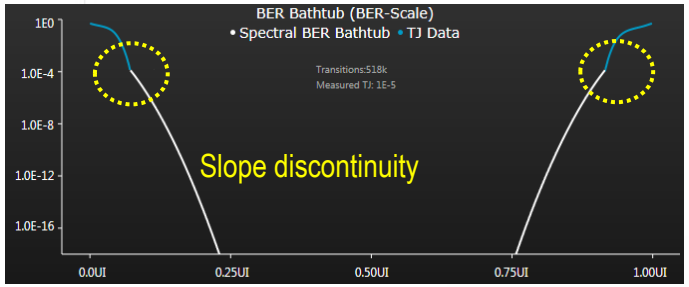
AMPLITUDE INTERFERENCE UNCORRELATED WITH DATA AND NOT PERIODIC

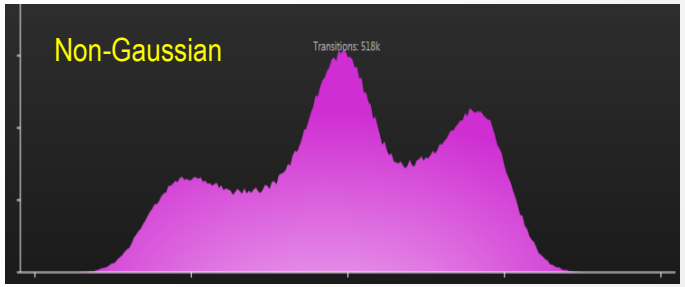






No crosstalk
Bathtub and RJ,PJ Histogram



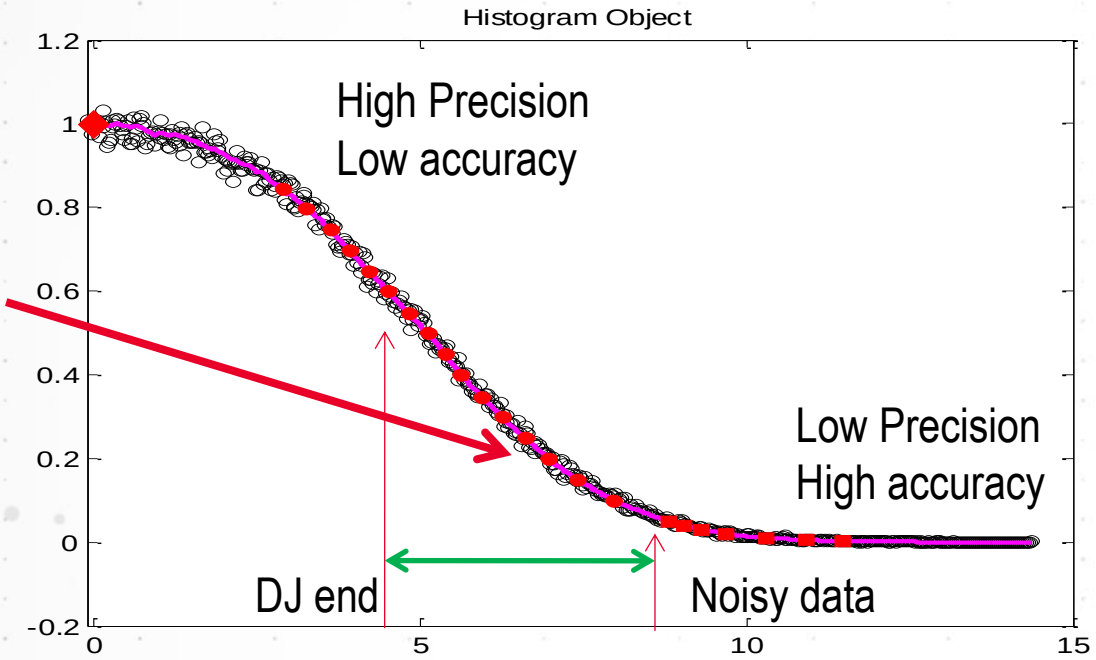


With crosstalk
Bathtub and RJ,PJ Histogram

What Makes Tail Fit Hard

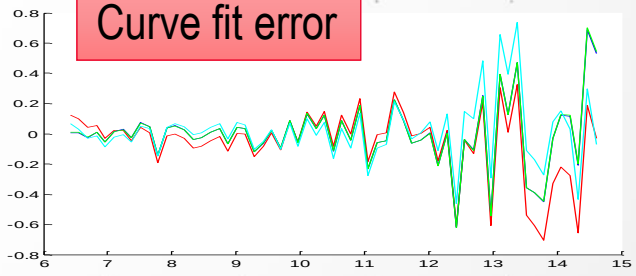
MEASUREMENT DETAIL

Fit Window



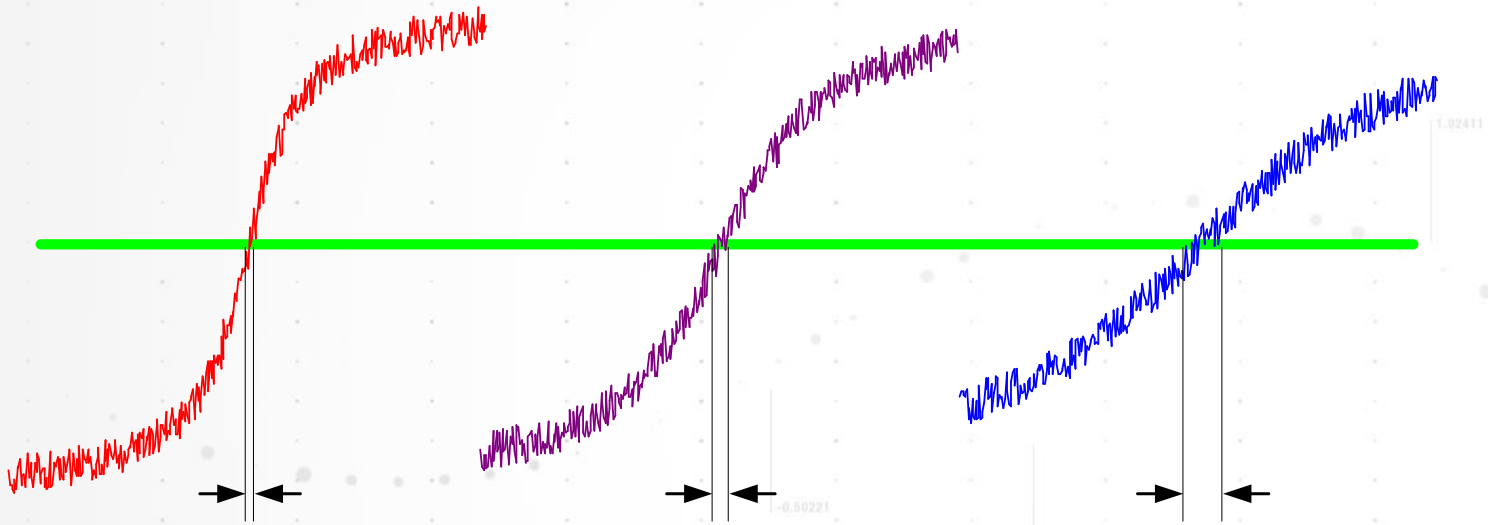
Hard to detect Crosstalk events out in the tail. Might take longer time for Tail Fit results to converge.

Curve fit error



Influence of Scope Noise to Jitter Performance

RANDOM JITTER WILL VARY WITH SLEW RATES.



TIE:

$$\sqrt{\left(\frac{Noise}{SlewRate}\right)^2 + SampleClockJitter^2} \quad \text{sec rms}$$

Periodic Jitter:

$$\sqrt{2} \cdot \sqrt{\left(\frac{Noise}{SlewRate}\right)^2 + SampleClockJitter^2} \quad \text{sec rms}$$

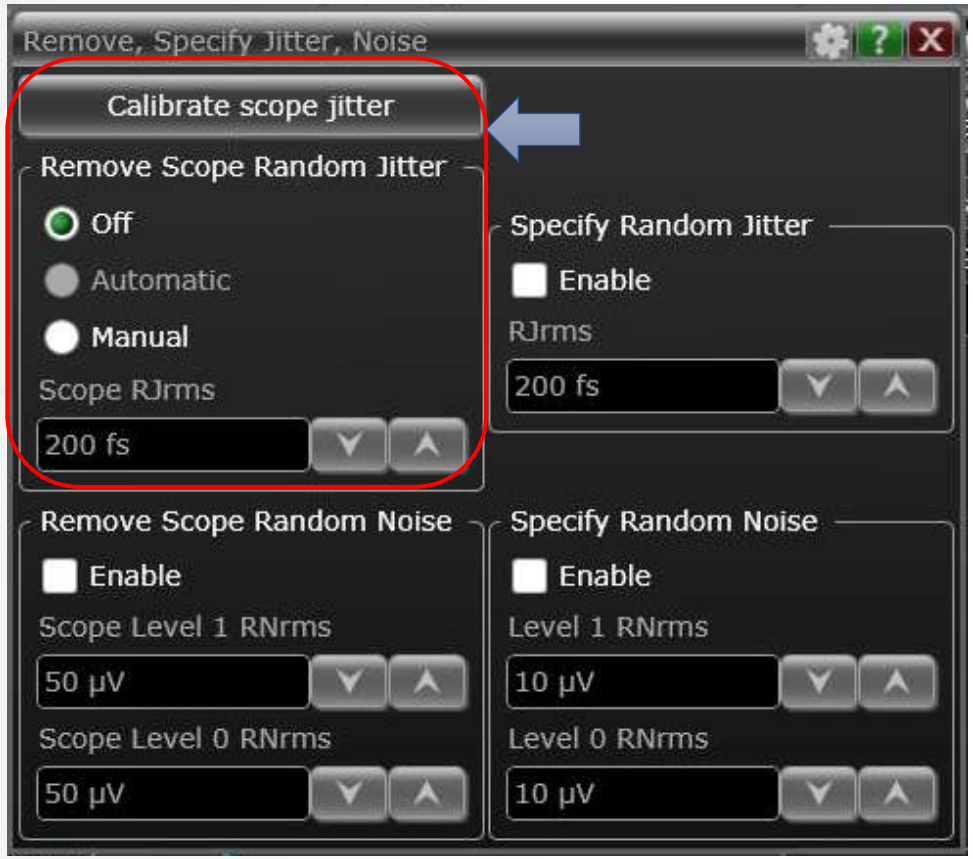
Cycle-Cycle:

$$\sqrt{3} \cdot \sqrt{\left(\frac{Noise}{SlewRate}\right)^2 + SampleClockJitter^2} \quad \text{sec rms}$$

1. Every scope has intrinsic vertical noise floor. This vertical noise can translate into horizontal jitter.
2. As signal slew rate decreases, vertical noise increases the random jitter.
3. Measured random jitter is a function of signal slew rate, scope noise and scope sample clock jitter.

Scope Random Jitter Removal

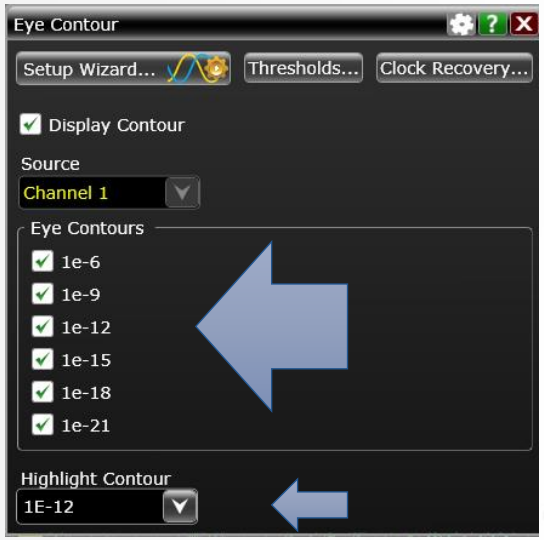
CALIBRATE AND REMOVE SCOPE RANDOM JITTER CONTRIBUTION



- Scope RJ calibration is available to remove the contribution of scope noise to measured RJ.
- User is asked to disconnect the signal from Channel to measure the ACV_{rms} noise for the current Vertical setting.

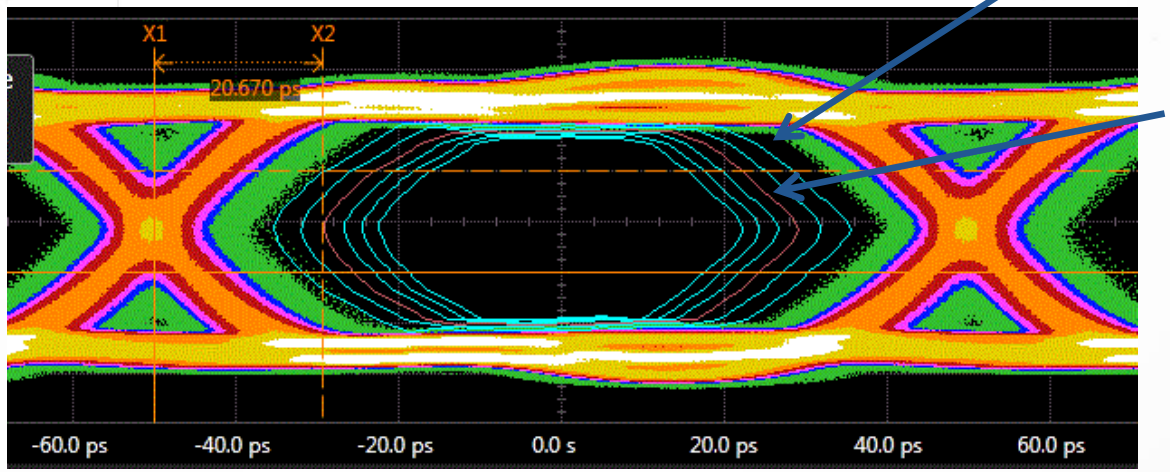
Jitter Analysis with BER Eye Contour

ESTIMATE JITTER AND EYE OPENING TO VARIOUS BER LEVEL



– Specify the BER eye contours you want the scope to plot.

– Specify which BER contour to highlight in red.

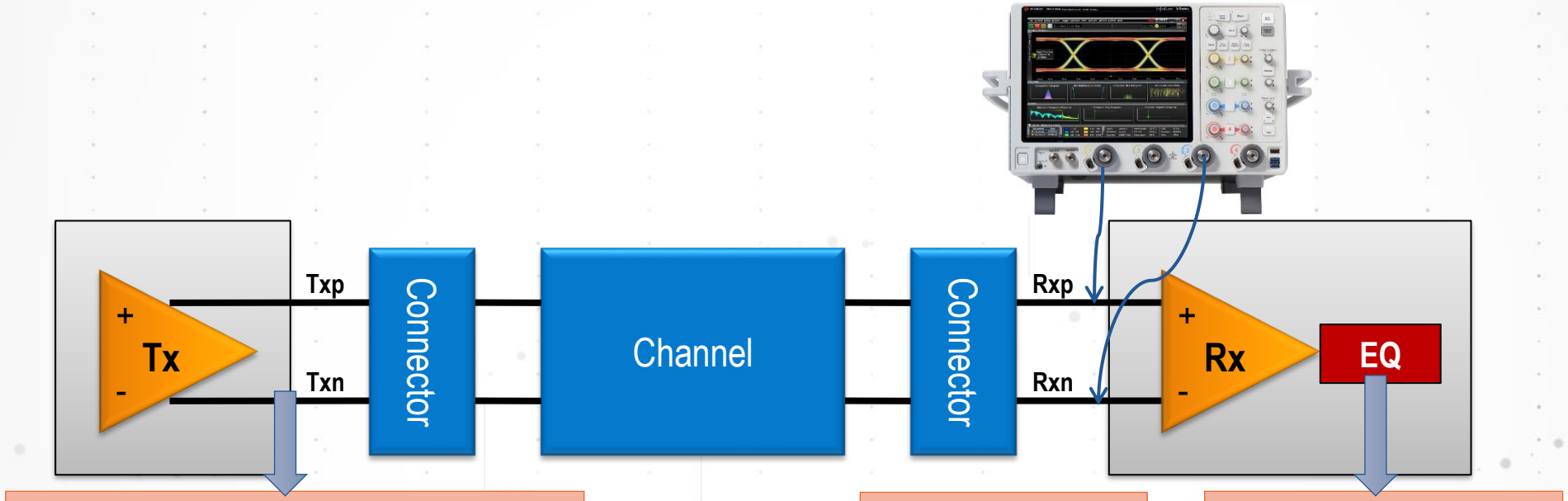


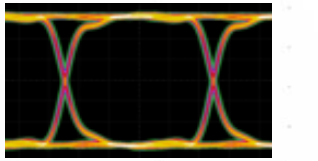
BER Eye Contours

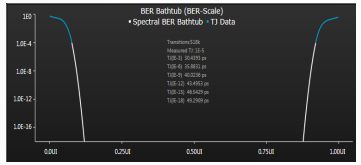
Eye Contour at BER 10^{-12}

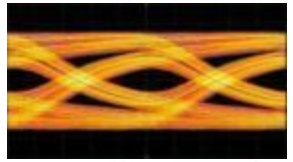
Analyze Jitter at Various Test Points

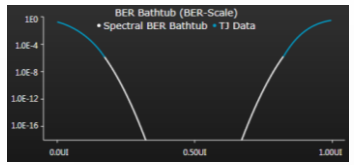
JITTER ANALYSIS WITH DE-EMBEDDING AND EQUALIZATION

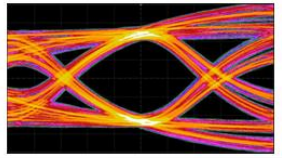




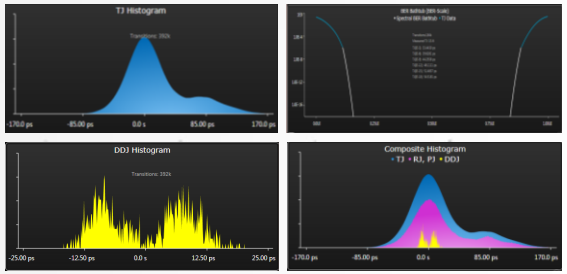




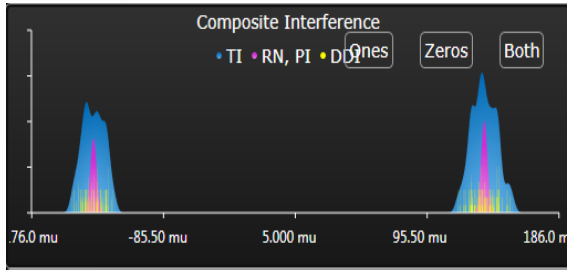




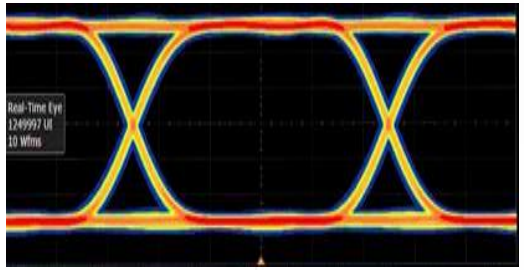
Keysight Real-Time Scope Jitter Analysis Tools



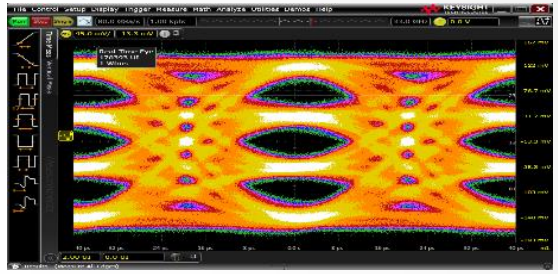
N5400A EZJIT Plus for Jitter Analysis and RJ Scope Removal Calibration



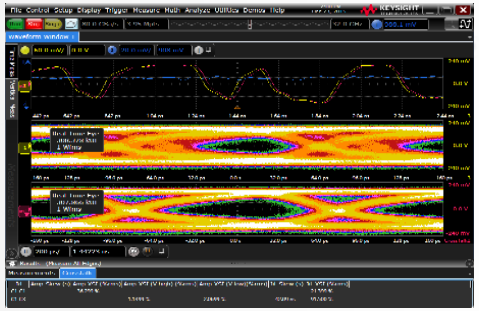
N8823A EZJIT Complete for Vertical Noise Analysis



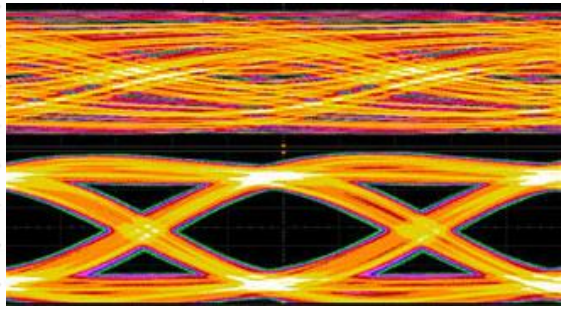
E2688A High-Speed SDA for Reference Clock Recovery and Eye Analysis



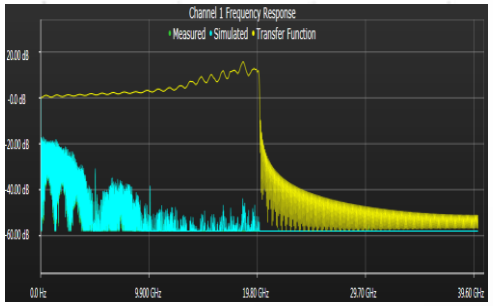
N8827A PAM-4 Clock Recovery



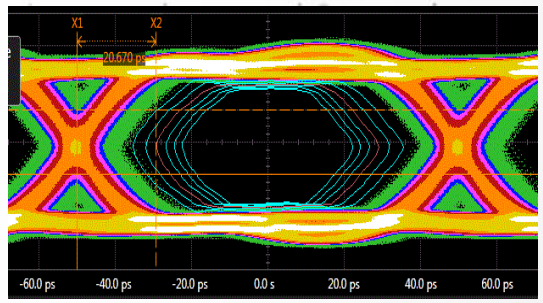
N8833A Crosstalk Analysis and Removal Application



N5461A Serial Data Equalization Software



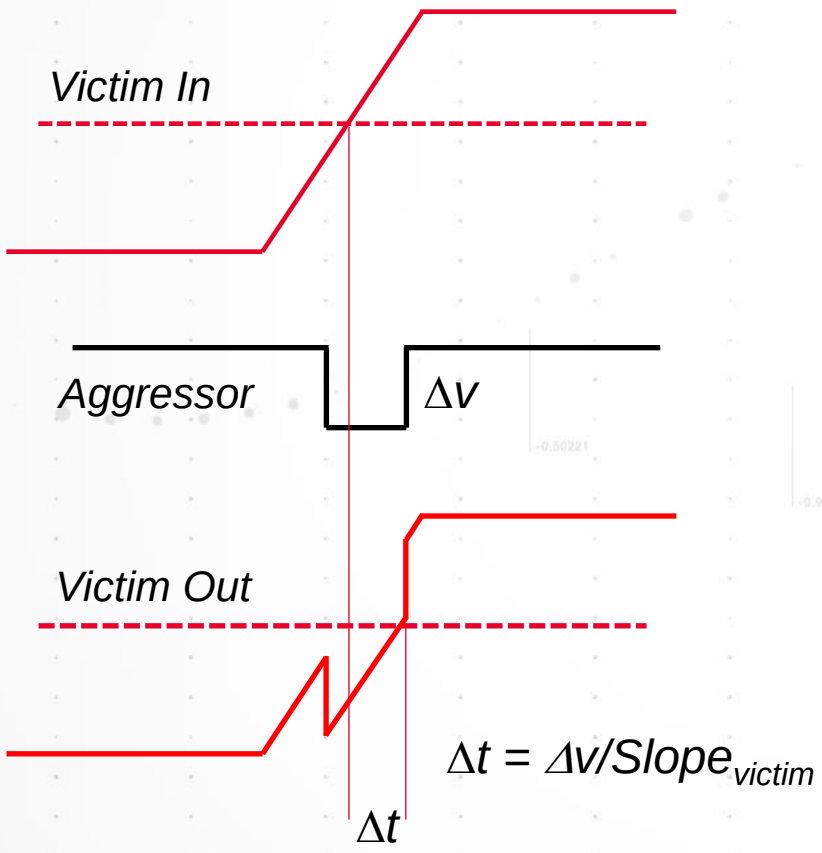
N5465A InfiniiSim De-embedding Software



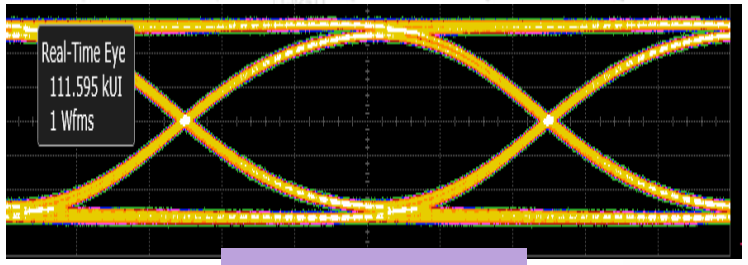
BER Eye Contour Comes standard with E2688A and N8823A

Crosstalk Overview

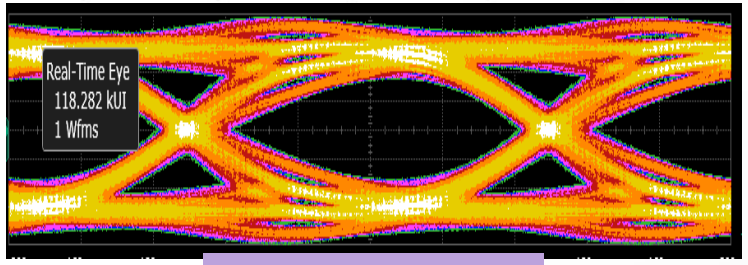
AMPLITUDE INTERFERENCE UNCORRELATED WITH DATA PATTERN



Impact on Eye

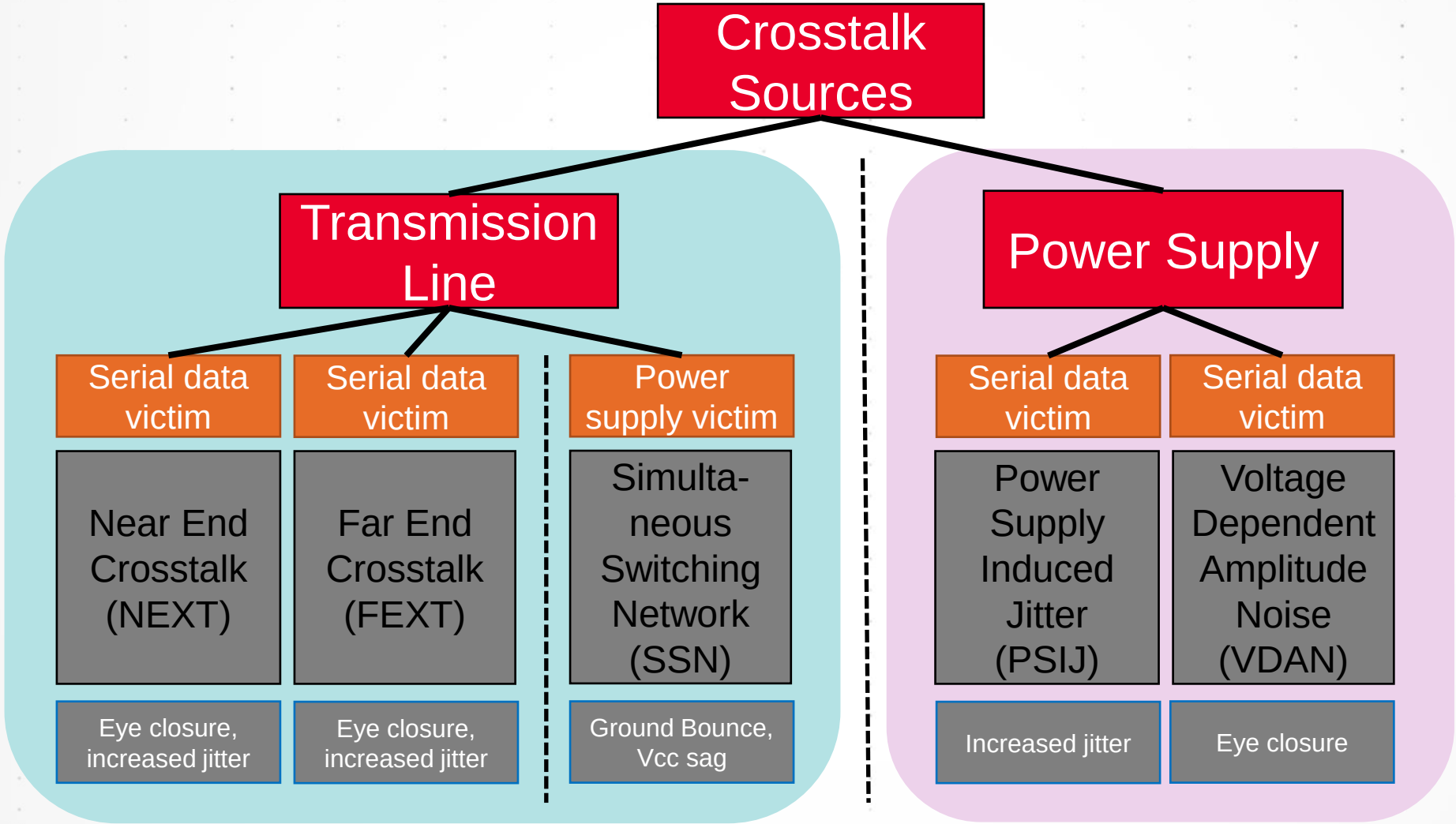


No crosstalk



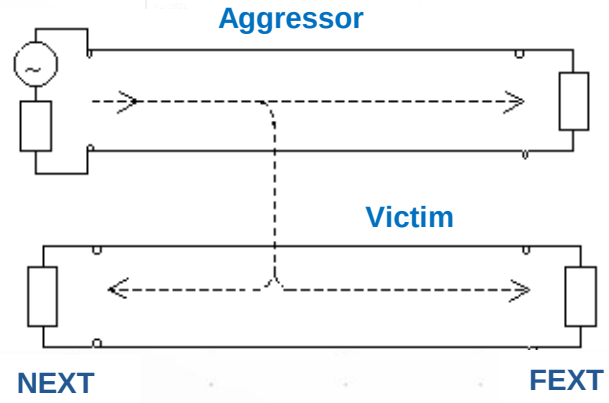
With crosstalk

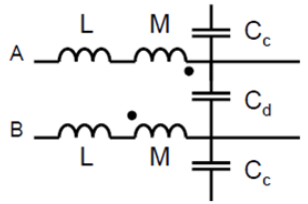
Sources of Crosstalk



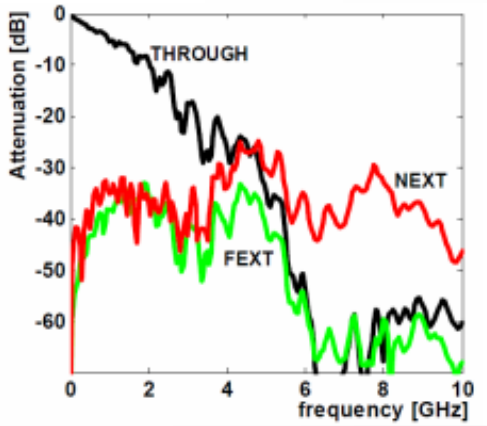
Transmission Line Crosstalk

- Crosstalk is becoming a more important issue, as data speeds increase, and more lanes are packed into small spaces. For example:
  - 100G standards with 4 parallel 25 Gb/s lines
  - ASICS with 100's of SerDes
- Transmission line crosstalk is the result of electromagnetic interference between electrical components.
- Mainly caused by capacitive or inductive coupling between multiple signal lines.
- Two prominent types:
  - Far End Xtalk (FEXT)
  - Near End XTalk (NEXT)





Mutual Inductance and Capacitance between 2 transmission lines.



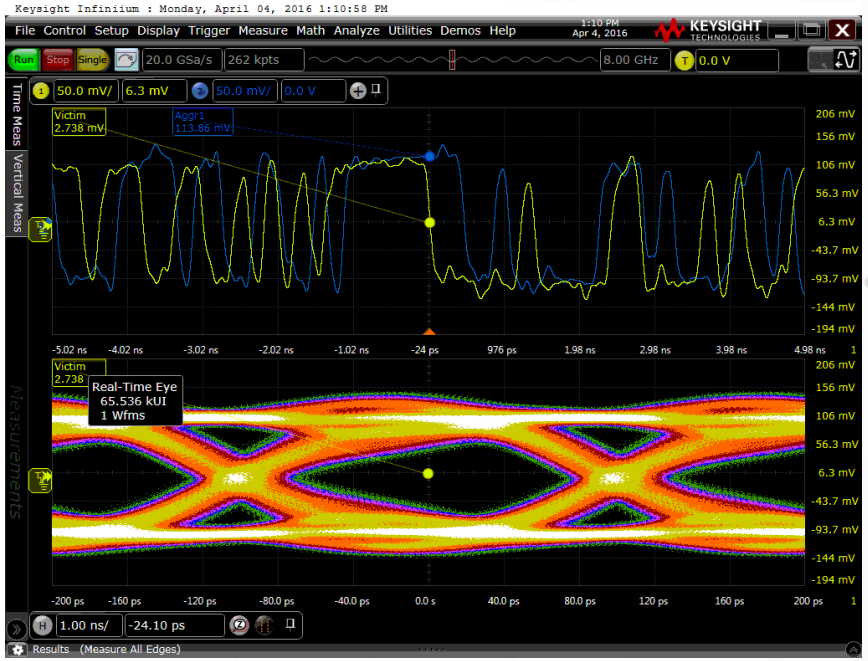
Transfer function examples for insertion loss, NEXT and FEXT

Far-End Crosstalk (FEXT)

No Serial Aggressor

FEXT Serial Aggressor

Aggressor traveling the same direction of Victim



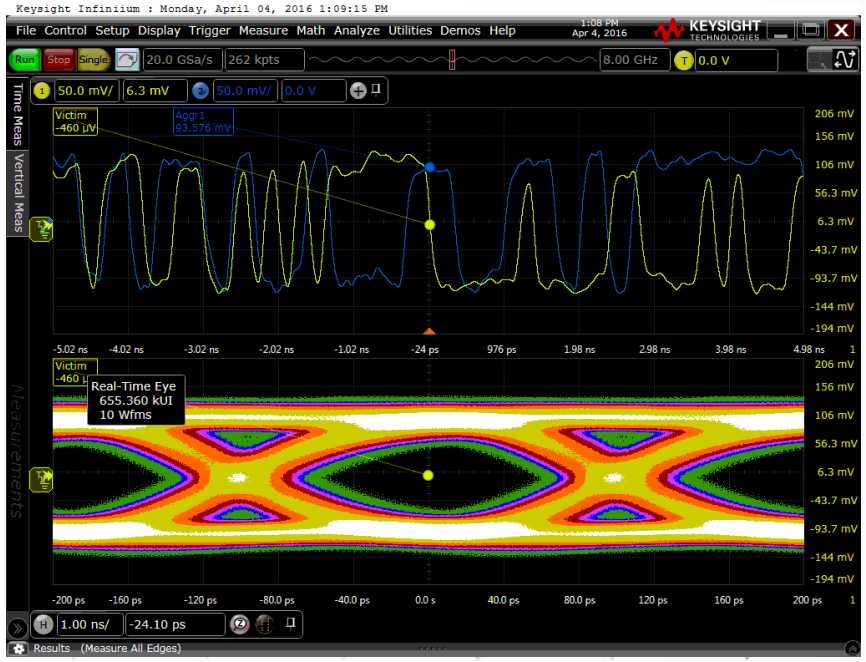
When data rate and pattern of the aggressor, and victim are the same, the eye diagram of the victim will show a bulging indicative of FEXT.

Near End Crosstalk (NEXT)

No Serial Aggressor

NEXT Serial Aggressor

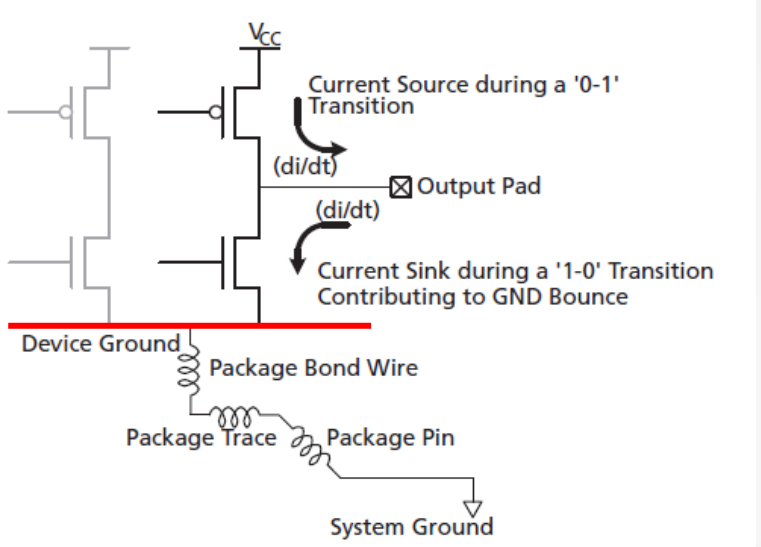
Aggressor traveling the opposite direction of Victim



NEXT distortion on the victim eye diagram appears to be more smeared out.

Power Supply Victim

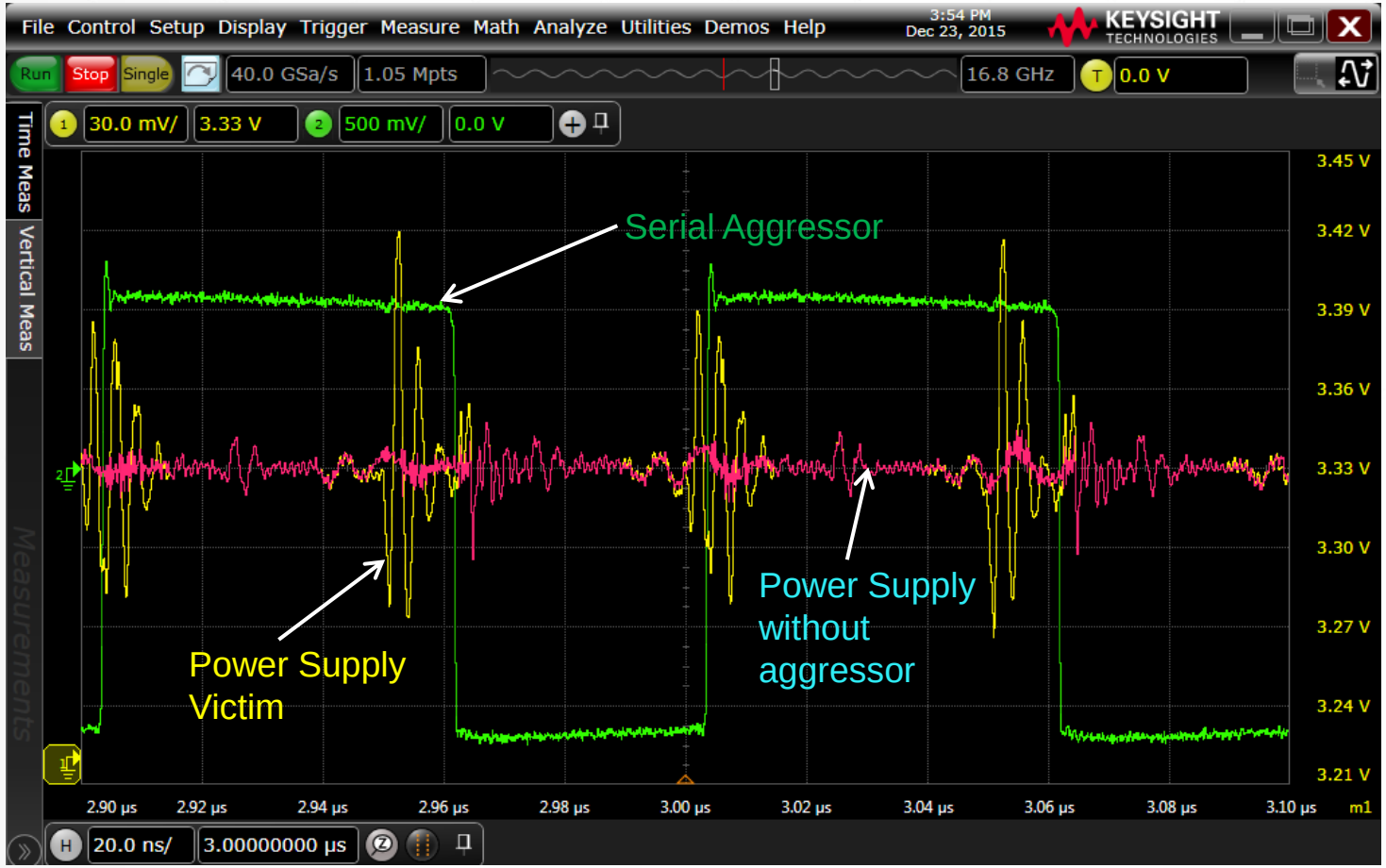
- A power supply can also be a victim, where the serial data lines are the aggressors. The best example is Simultaneous Switching Noise (SSN) which can create Ground Bounce (the high voltage rail can also “bounce” and may be referred to as V_{cc} sag).
- SSN is the result of parasitic inductances that lie between the device (chip) ground and the system (board) ground. When a serial data line switches states, current flows through these inductances which produces a voltage drop. The more lines that switch at the same time (simultaneously) the bigger the drop.



A simplified circuit showing the parasitic inductances that contribute to Ground Bounce. The Ground Bounce effect can propagate to other circuits via device ground, affecting other signals.

Power Supply Victim

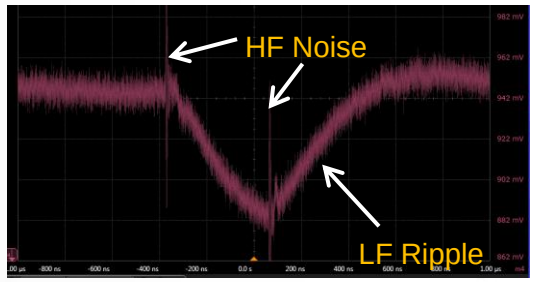
EXAMPLE OF POWER SUPPLY VICTIM DUE TO CLOCK EDGES



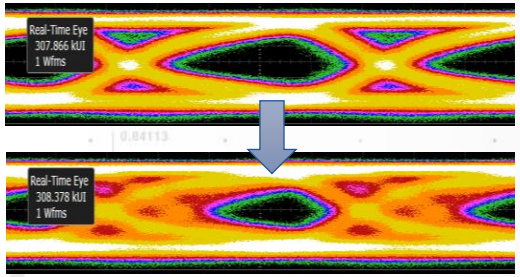
Note the large ringing in the yellow power supply that is correlated with the edges of the clock.

Power Supply Aggressors

- Power Supply Induced Jitter (PSIJ) – Adds jitter through PLL power supply



Noise in the power supply closes the eye horizontally.



- Voltage-Dependent Amplitude Noise (VDAN) – Adds noise to logic level 0 & 1 via voltage references

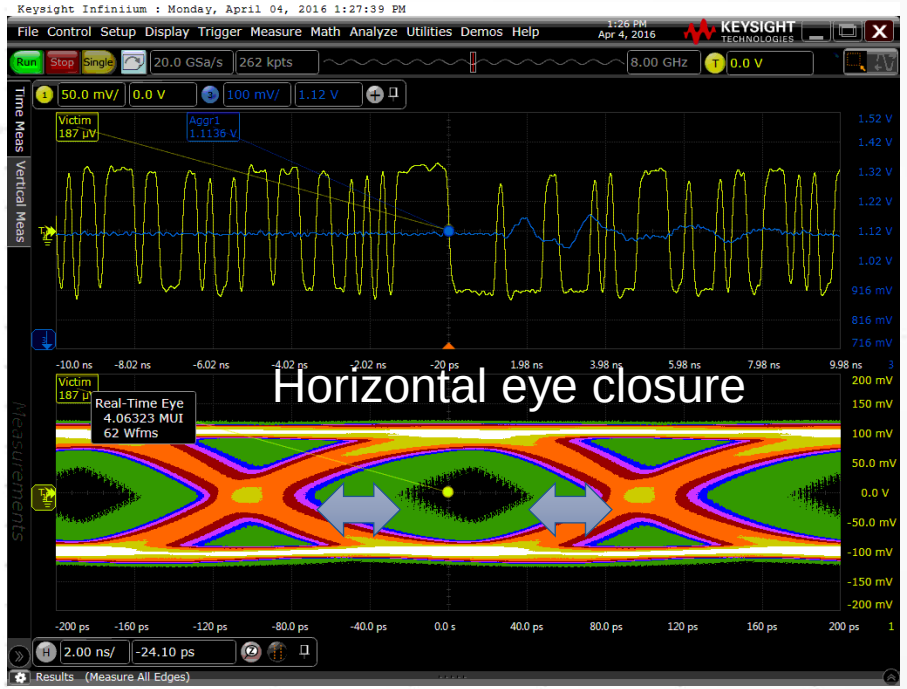
Noise on Vcc, logic high voltage reference is transferred to logic high bits, but not affecting the logic low bits that references the ground.

Power Supply Aggressor – PSIJ

POWER SUPPLY INDUCED JITTER

No Power Aggressor

With PSIJ Aggressor



High frequency noise in the power supply, induces horizontal jitter.

Power Supply Aggressor – VDAN

VOLTAGE DEPENDENT AMPLITUDE NOISE

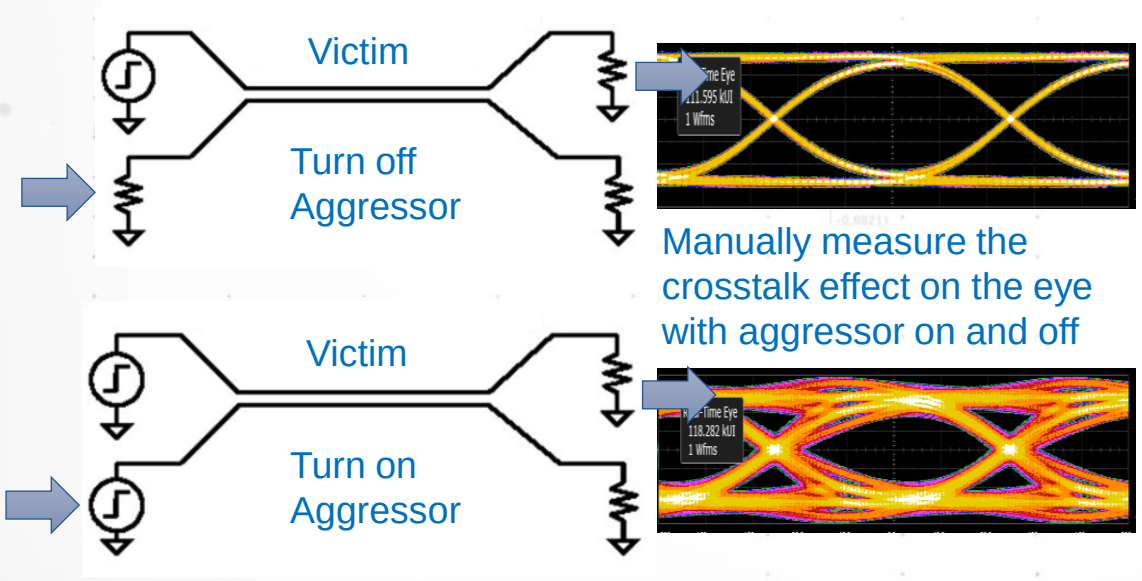
No Power Aggressor

With Power VDAN Aggressor

Changes (noise) in V_{cc} level is coupled into the logic high and low bits.

Legacy Method of Measuring Crosstalk

- The need to troubleshoot and characterize crosstalk is not new, but the legacy methods of measuring crosstalk in digital communications systems has relied on the process of selectively disabling some channels while enabling others.
- This necessarily requires measuring the crosstalk effects in the system while operating in special test modes, which means measuring them under abnormal conditions. Worse yet, some systems cannot even operate the necessary special modes.



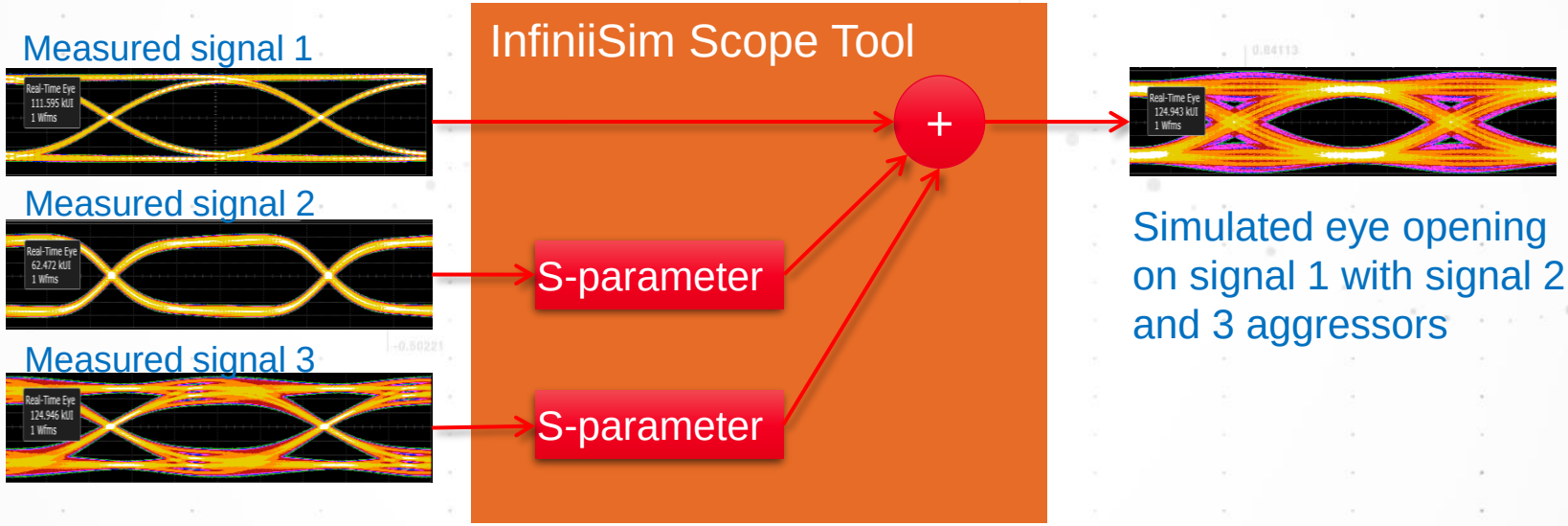
Manually measure the crosstalk effect on the eye with aggressor on and off

Challenges:

- No special test modes to turn on and off aggressors.
- Huge effort and time to characterize crosstalk from multiple serial aggressors.
- Power supply cannot be turned off.

Crosstalk Simulation, but not Identification or Removal

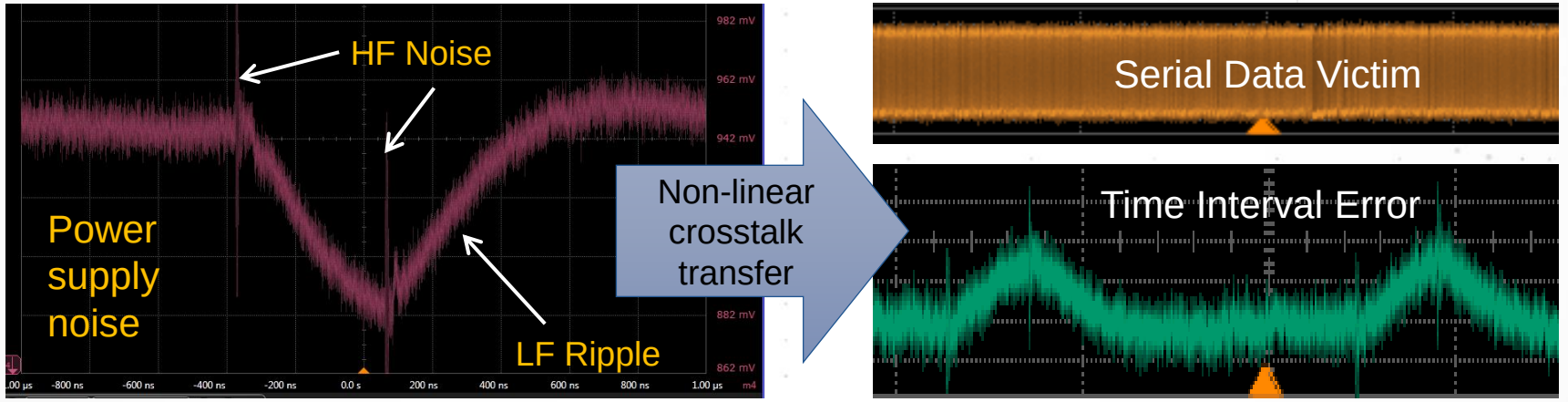
- Vector Network Analyzer (VNA) can be used to characterize crosstalk between serial data lines. S-parameter models are generated by the VNA.
- Scope and software tools are available today, using the S-parameter models to simulate the waveform distortion, eye closure and jitter performance.



- This method is *limited only to simulation and requires known sources of crosstalk.*
- However, it is unable to identify the real source of crosstalk on the real system or remove crosstalk from the measured waveforms for analysis to see how much margin can be recovered.

Power Supply, Non-Linear Crosstalk

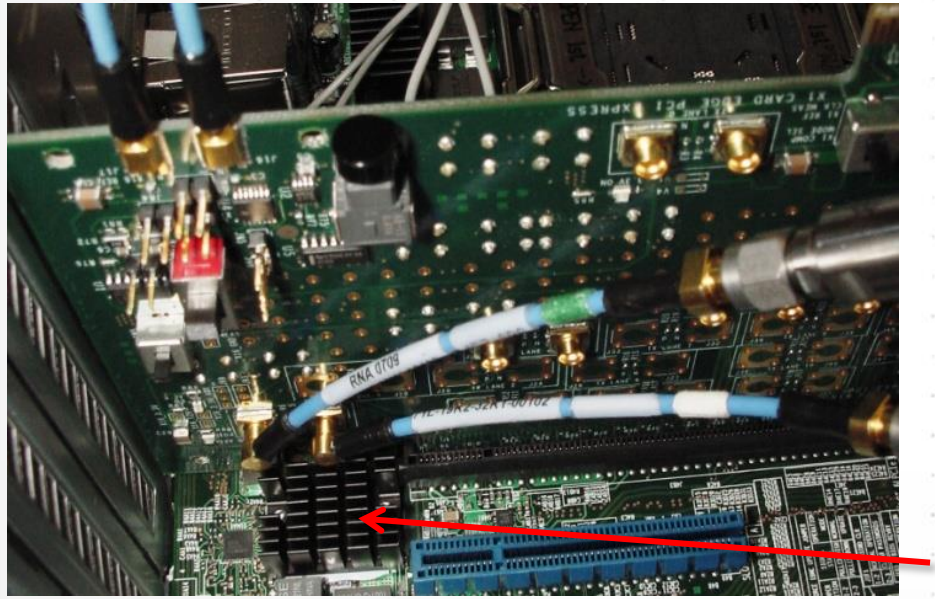
- For serial data lines, VNA can be used to characterize crosstalk because they are linear network model.
- However, the influence of power supply noise to serial data jitter and amplitude distortion is non-linear and there is no easy way to characterize the crosstalk transfer.



Power supply noise creates a non-linear transfer on the serial data timing error. The crosstalk transfer is difficult to solve and correlate.

Inaccessible Aggressor Signals

- Crosstalk could happen inside a silicon package with accessibility only to the serial data output.
- High density backplane connectors and switches are susceptible to crosstalk and difficult to access the signals to narrow down the source of crosstalk.
- Is there a way to characterize or debug such crosstalk scenarios?



Package with only TX output

Many crosstalk issues happen inside the package. How to troubleshoot crosstalk when the aggressors are inaccessible?

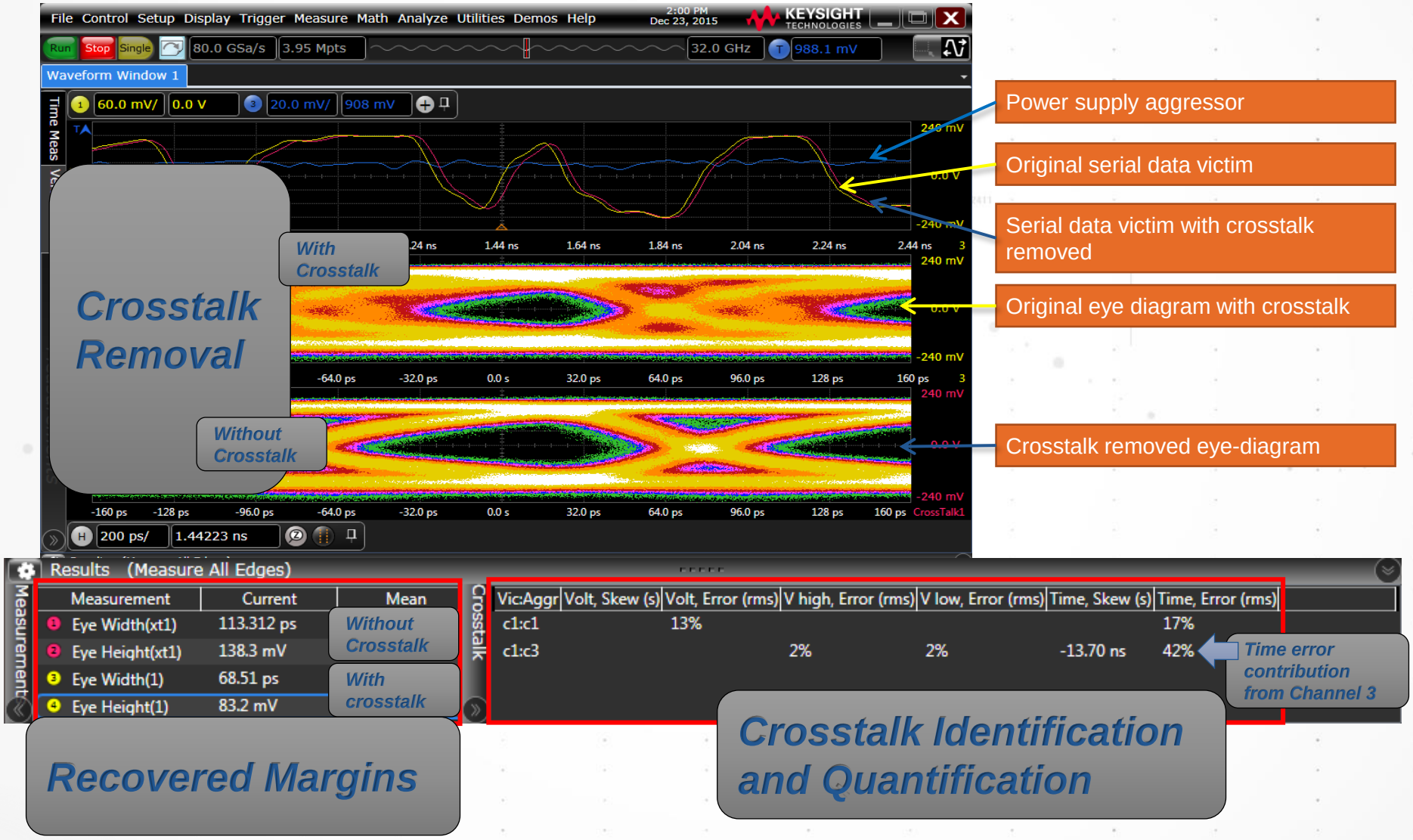
Crosstalk Analysis Challenges Solved by Application

- Crosstalk Identification
  - Which signals are coupling onto your victim?
- Crosstalk Quantification
  - How much error does each aggressor add to your victim?
- Crosstalk Removal for Analysis
  - What would your signal look without crosstalk?
  - How much margin can be recovered on your signal without crosstalk?
  - If the signal was failing spec, can it pass without crosstalk?

Assist in making important design decisions:

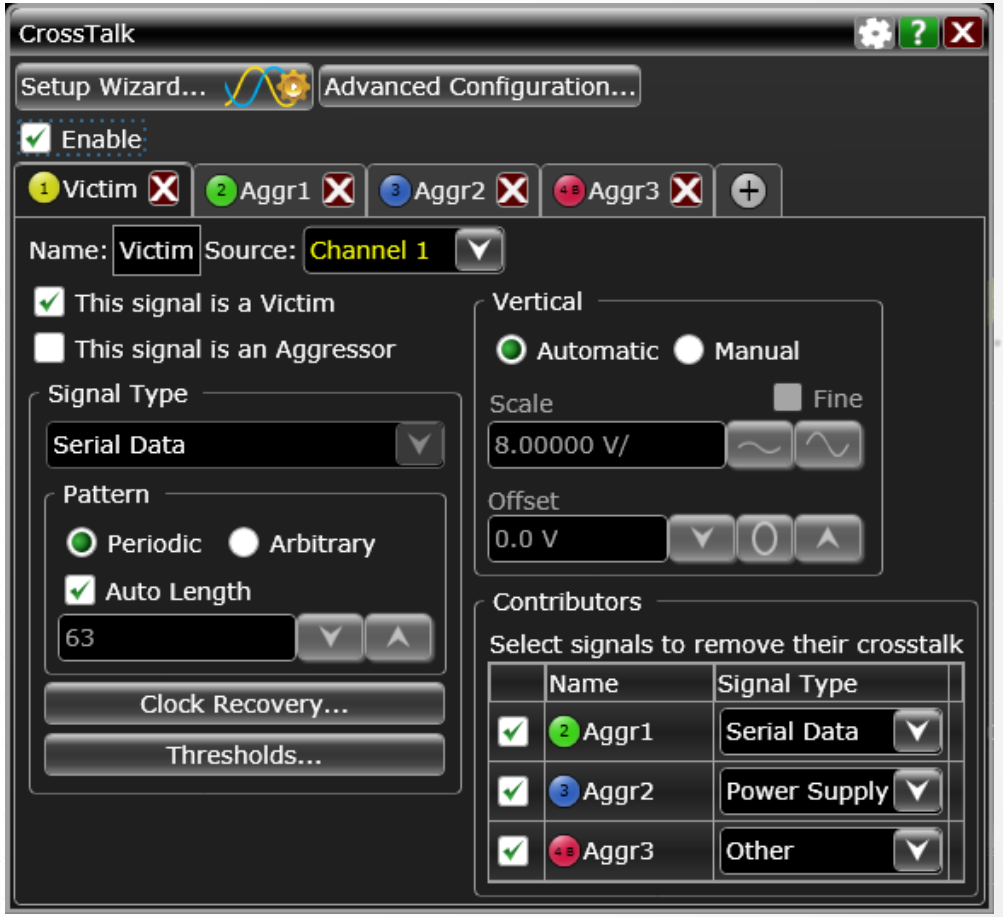
- ***Is it worth reducing crosstalk impact in design?***
- ***Where to improve?***

Challenges Solved by the Crosstalk Application



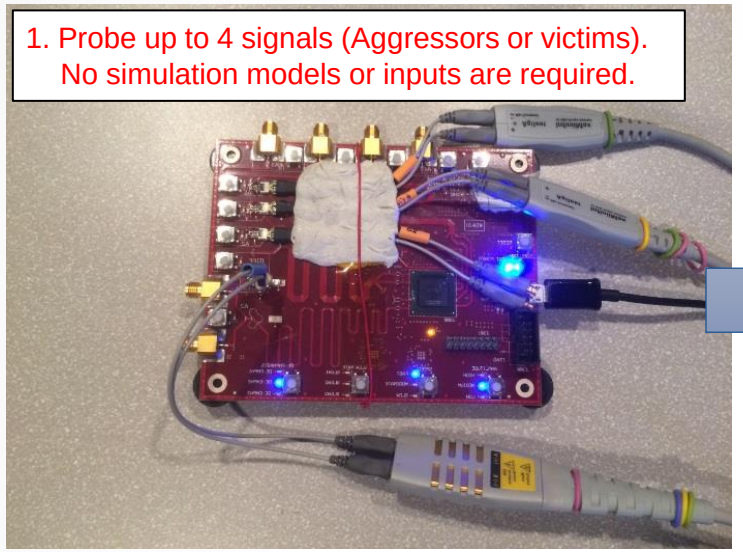
Features of the N8833A/B Crosstalk Analysis Application

1. Analyze up to four signals (victim or aggressor) at once. Any scope channels can be chosen as a victim or aggressor.
2. No crosstalk model or simulation files required
3. Identify aggressors using a browser probe. Use a solder-in probe for a more secure connection.
4. Report the amount of crosstalk present on victims
5. Work for both NEXT and FEXT, automatically determined by the app
6. Work for power supply analysis
7. Plot waveform without crosstalk on the scope which can be:
   - Used for eye diagram, jitter decomposition, de-embedding, equalization and mask test
   - Saved as a waveform file

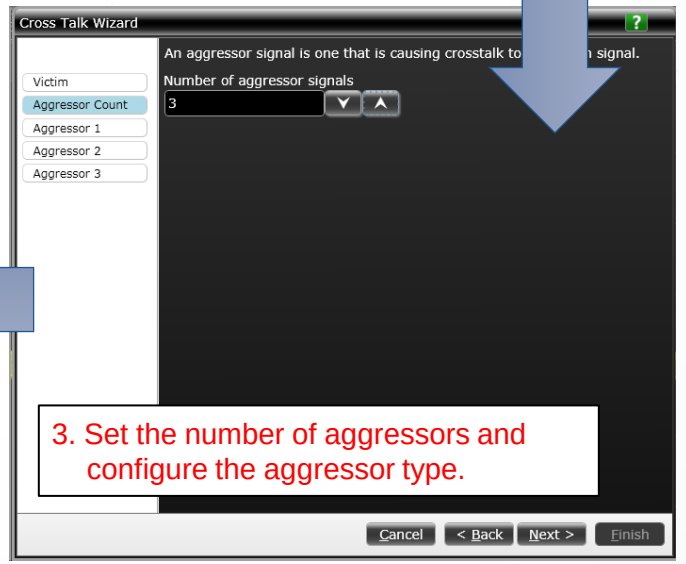


Crosstalk Analysis Setup

1. Probe up to 4 signals (Aggressors or victims). No simulation models or inputs are required.

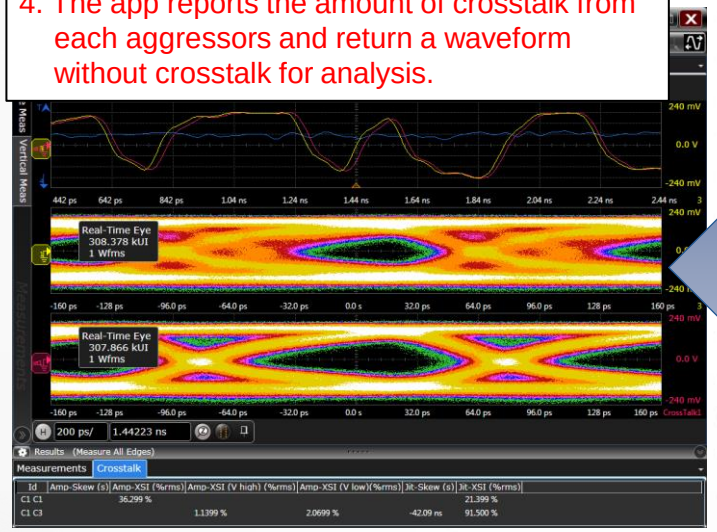


2. Setup the victim signal.



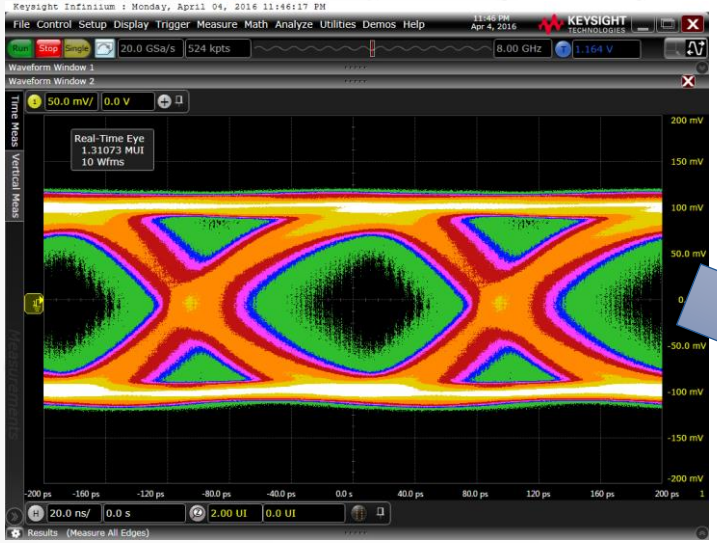
3. Set the number of aggressors and configure the aggressor type.

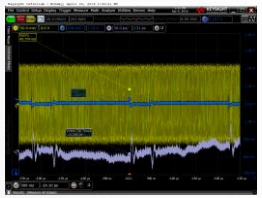
4. The app reports the amount of crosstalk from each aggressors and return a waveform without crosstalk for analysis.

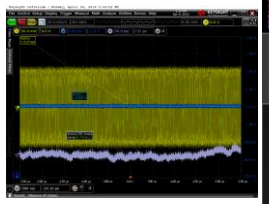


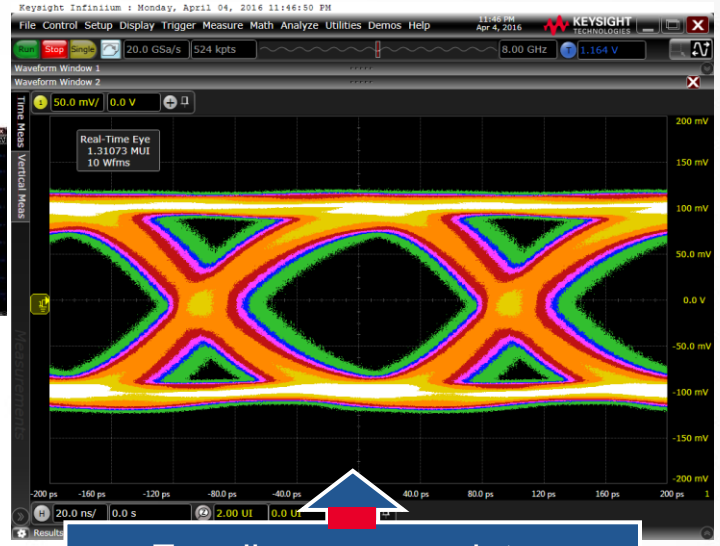
Example: Removing Power Supply Crosstalk

Measured Victim with Power Supply Crosstalk



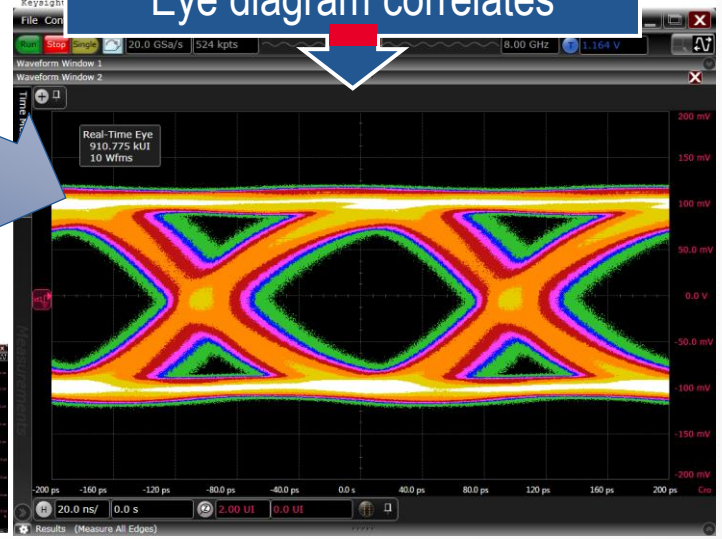


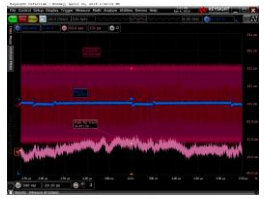




Measured Victim Without Crosstalk

Eye diagram correlates





Victim after Power Supply Crosstalk removed

Example: Jitter Improvement Without Power Supply Crosstalk

COMPARE JITTER RESULTS BEFORE AND AFTER CROSSTALK REMOVAL.

TJ = 158ps
PJdd = 58ps
DJdd = 68ps

An Improvement of 20% to Total Jitter without Crosstalk.

TJ = 124ps
PJdd = 27ps
DJdd = 33ps

Universal Serial Bus (USB)

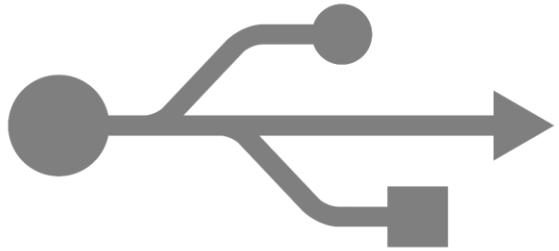
Buzzwords categorized

Specifications

USB 3.0 → USB 3.1 → **USB 3.2**
USB4 → **USB4 Version 2.0**

USB-C

Connector form factor
Specification



PHY Bit Rates Per Lane

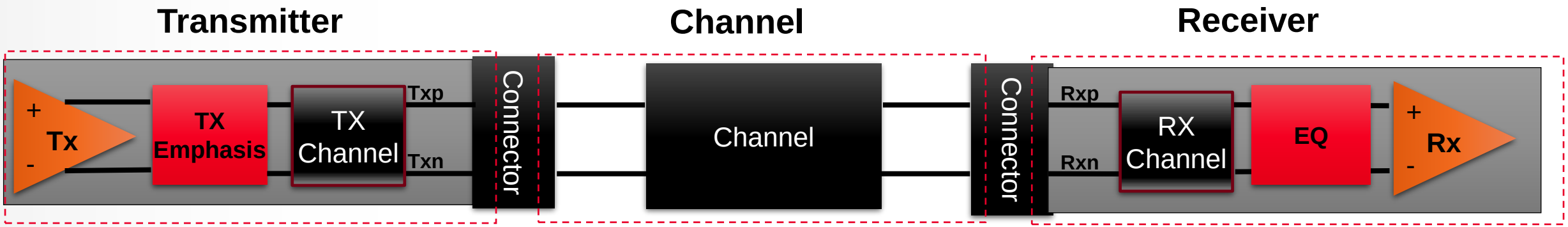
Gen1	5 Gb/s
Gen2	10 Gb/s
Gen3	20 Gb/s
Gen4	40 Gb/s

Marketing Terms

Super Speed = Gen1
Super Speed Plus = Gen2

Typical Digital Communication Link Physical Layer (PHY)

TRANSMITTER (TX), CHANNEL AND RECEIVER (RX)



Real-time Oscilloscope (UXR)

Equivalent-time Oscilloscope (DCA)

Network Analyzer (PNA, ENA)

TDR/TDT (DCA)

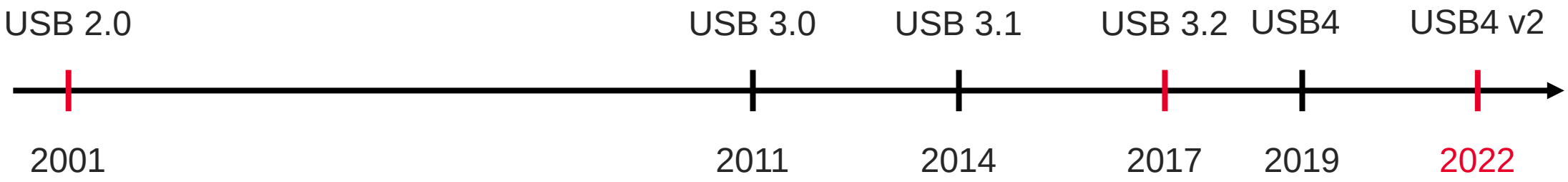
Bit Error Ratio Tester (BERT), Pattern Generator (PG)

Universal Serial Bus (USB) Specifications

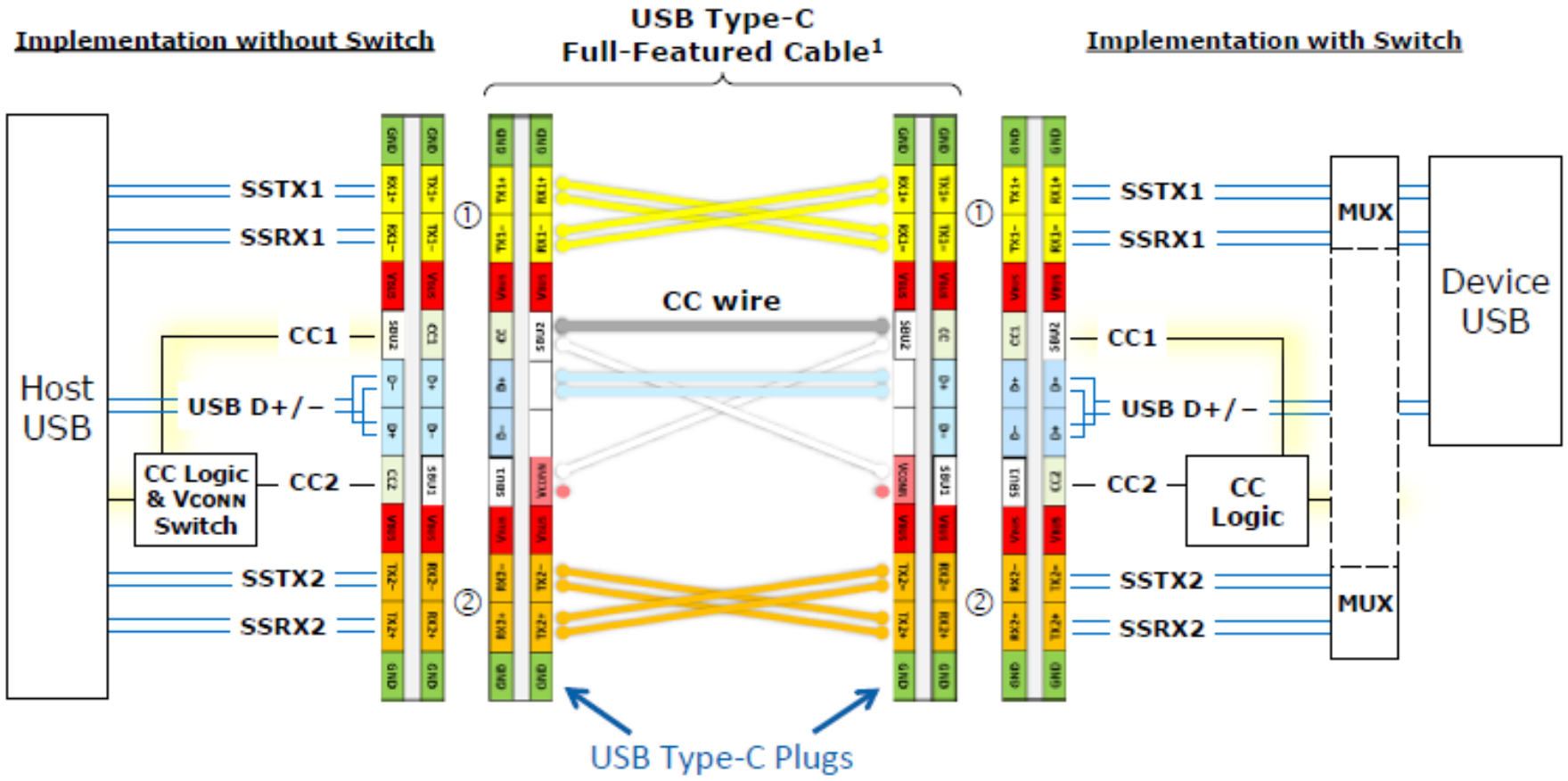
- **Spec version ≠ PHY data rate**
- Three specifications are active
  - USB 2.0
  - ~~USB3.0~~ → ~~USB 3.1~~ → USB 3.2
  - ~~USB4~~ → USB4 Version 2.0

USB 2.0	USB 3.0	USB 3.1	USB 3.2	USB4	USB4 v2
1.5 Mb/s 12 Mb/s 480 Mb/s	5 Gb/s	5 Gb/s 10 Gb/s	5 Gb/s x1 10 Gb/s x1 5 Gb/s x2 10 Gb/s x2	10 Gb/s x2 20 Gb/s x2	10 Gb/s x2 20 Gb/s x2 40 Gb/s x 2 (25.6 GBd PAM3)

x2 = two physical channels bonded into one logical channel



Type-C Implementation Challenges

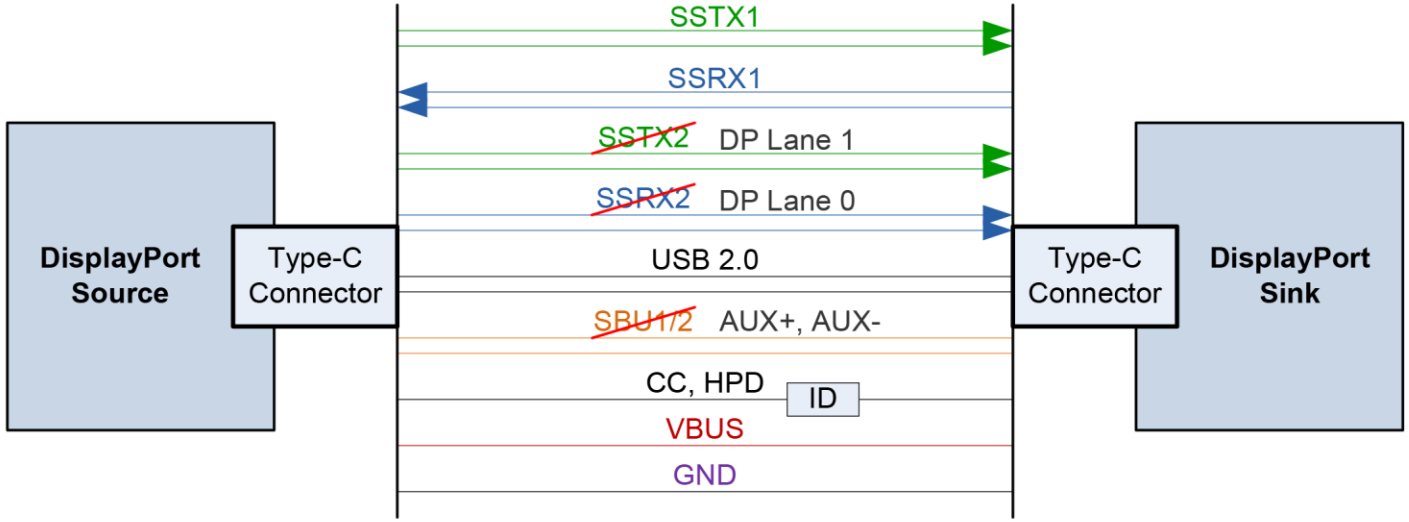


Diagrams courtesy USB-IF

Type-C Implementation Challenges

DisplayPort and USB 3.2 over a Type-C to Type-C Passive cable

Configuration for Docking Stations



- DisplayPort uses two high speed lanes
  - For DP 1.2a (HBR2), this provides support for 2560x1600 or 2 each 1080p displays
  - For DP 1.3 (HBR3), this will provide support of 4K UHD (3840 x 2160)
- Two high speed lanes used for USB 3.1
- USB 2.0 and USB Power Delivery always available

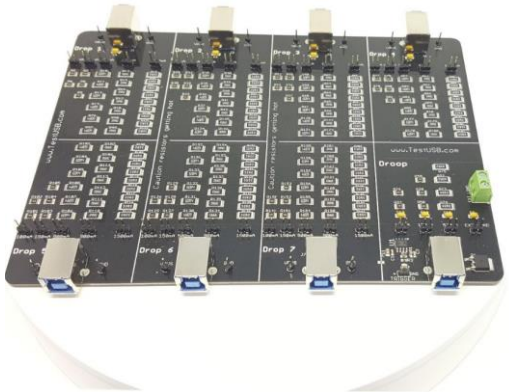
USB 2.0 Type-A/B Electrical Test Fixtures

From USB-IF: Allion or Fixture Solution

USB 2.0 Std-A/Std-B Electrical Test Fixtures

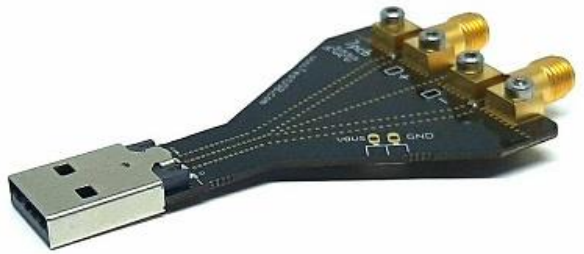
Fixtures can be purchased directly from Allion at https://www.allion.com/fixtures

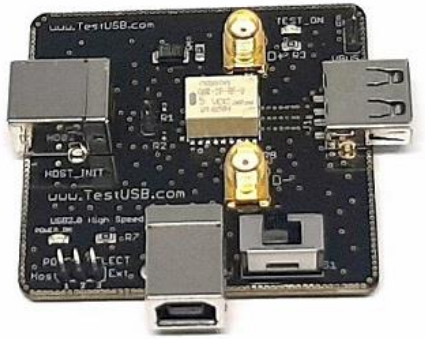
Fixtures can be purchased directly from Eurofins at http://testusb.com/shop.htm



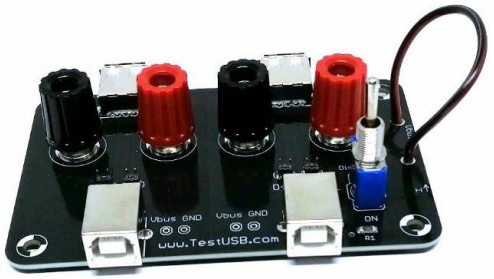
USB A High Speed Signal Quality Test Fixture Set

USB A TX Test Fixture





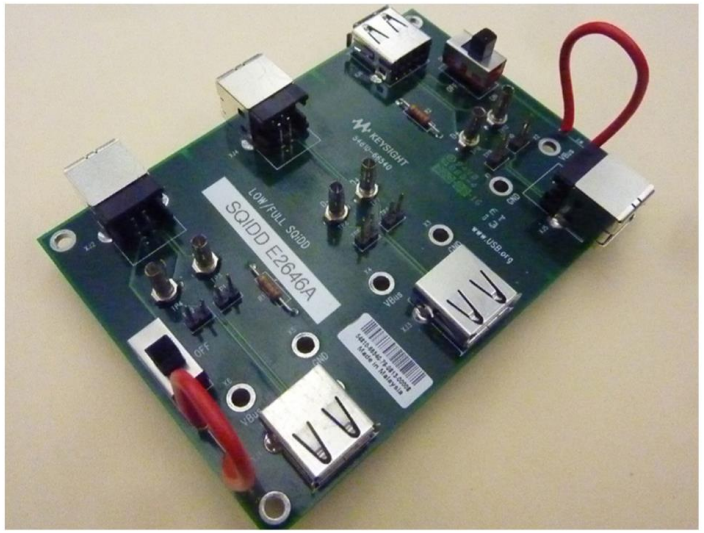
High-Speed Embedded Host Electrical Test Board



USB 2.0 Type-A/B Electrical Test Fixtures

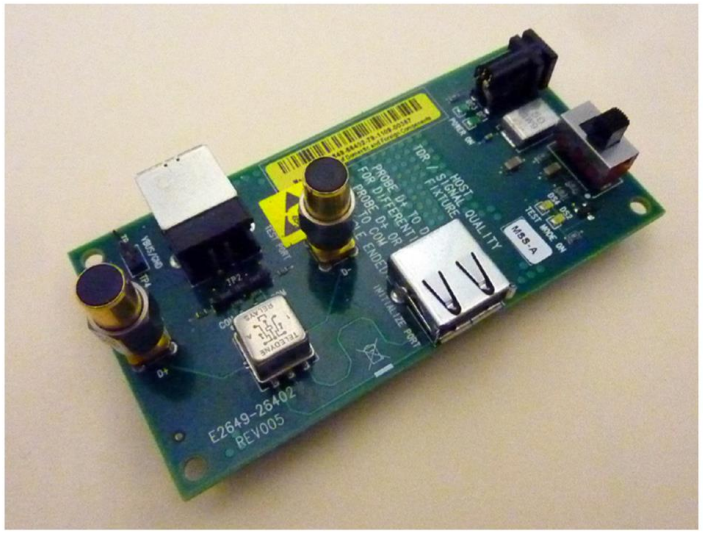
From Keysight

▶ **E2649B** USB 2.0 High-Speed Fixture Set



▶ **E2646B** "SQuIDD" test fixture for testing USB 2.0 low- and full-speed products

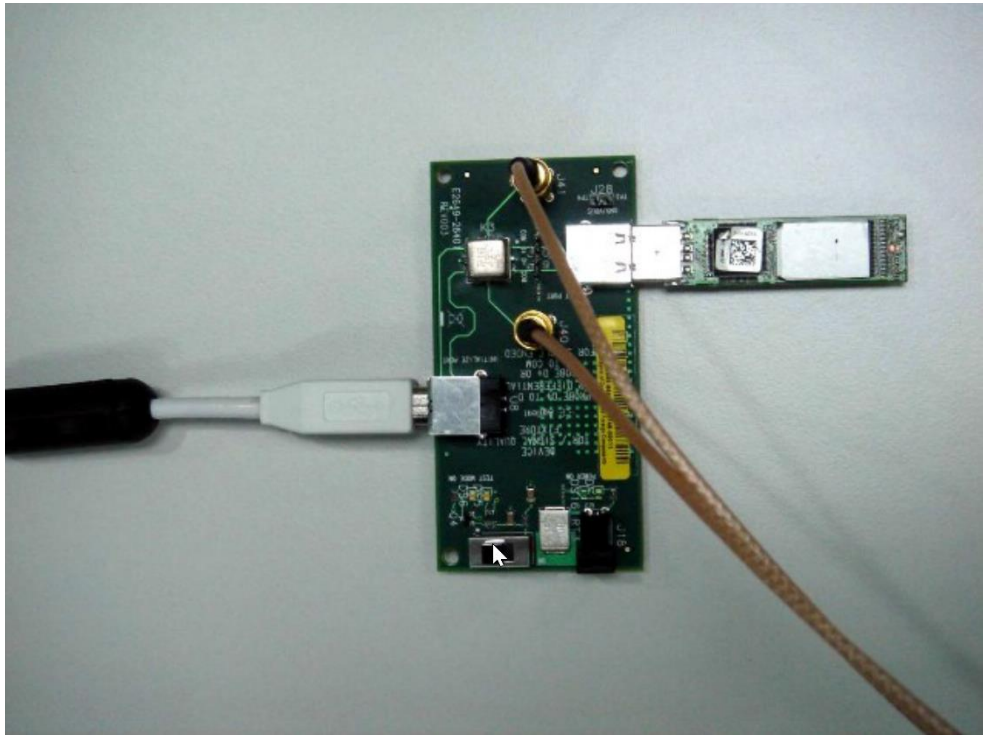
▶ **E2666B** hi-speed device test fixture



▶ **E2667B** hi-speed host test fixture

USB 2.0 Type-A/B Electrical Test Fixtures

From Keysight

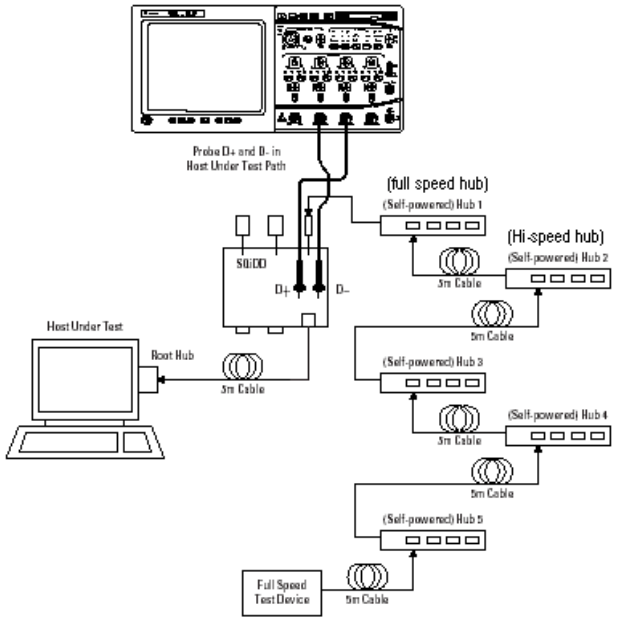


Single-Ended SMA Cable Connection
for Hi-Speed Signal Quality Tests

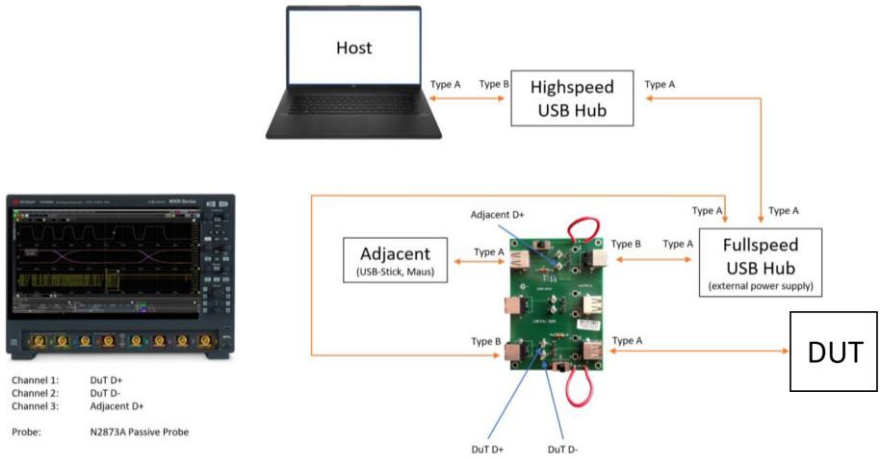
USB 2.0 Type-A/B Electrical Test Fixtures

From Keysight

- **Low and Full Speed** host tests require two single-ended probes.



- **Low and Full Speed** device tests require three single-ended probes — the third probe is for the adjacent D-/D+ signal.



- The **passive probes** that are included with the oscilloscope are sufficient.

N2873A Passive Probe, 10:1, 500 MHz, 1.3 m

Single-Ended Probe Connection for Full/Low-Speed Signal Quality Tests

FAQ

D9010USBC Frequently Asked Questions

1. **What is USBET20?**

   USBET20 is a stand-alone electrical signal analysis tool for USB Compliance testing. USBET20 is the official compliance electrical analysis tool that performs pass/fail assessments on signal quality and inrush current data captured from an oscilloscope.

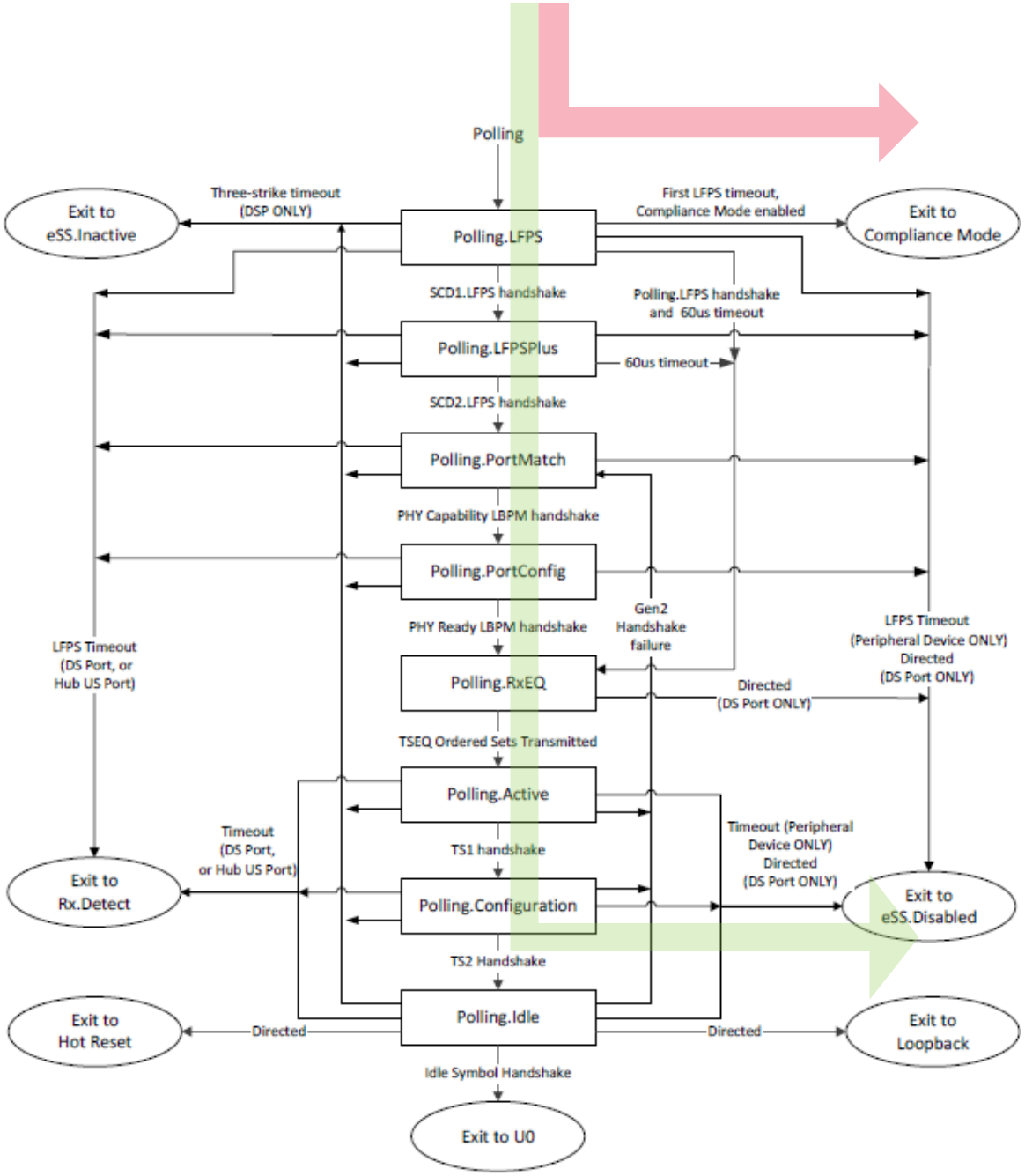
2. **What is XHSETT?**

   XHSETT (or USBHSET) is a tool used to generate test packets on the USB port under test. Latest versions available here: http://www.usb.org/developers/tools/

3. **Can we use USBET20 from past or future versions?**

   Yes, in the D9010USBC version 4.20 release onwards, it has the flexibility to use different USBET20 versions.

USB 3.2 LTSSM


Polling
Polling.LFPS
Three-strike timeout
(DSP ONLY)
Exit to
eSS.Inactive
First LFPS timeout,
Compliance Mode enabled
Exit to
Compliance Mode
SCD1.LFPS handshake
Polling.LFPS handshake
and 60us timeout
Polling.LFPSPlus
60us timeout
SCD2.LFPS handshake
Polling.PortMatch
PHY Capability LBPM handshake
Polling.PortConfig
PHY Ready LBPM handshake
Gen2
Handshake
failure
LFPS Timeout
(DS Port, or
Hub US Port)
LFPS Timeout
(Peripheral Device ONLY)
Directed
(DS Port ONLY)
Polling.RxEQ
Directed
(DS Port ONLY)
TSEQ Ordered Sets Transmitted
Polling.Active
Timeout
(DS Port,
or Hub US Port)
Timeout (Peripheral
Device ONLY)
Directed
(DS Port ONLY)
TS1 handshake
Exit to
Rx.Detect
Polling.Configuration
Exit to
eSS.Disabled
TS2 Handshake
Exit to
Hot Reset
Directed
Polling.Idle
Directed
Exit to
Loopback
Idle Symbol Handshake
Exit to U0

USB 3.2 Compliance Pattern (CP's) Sequences

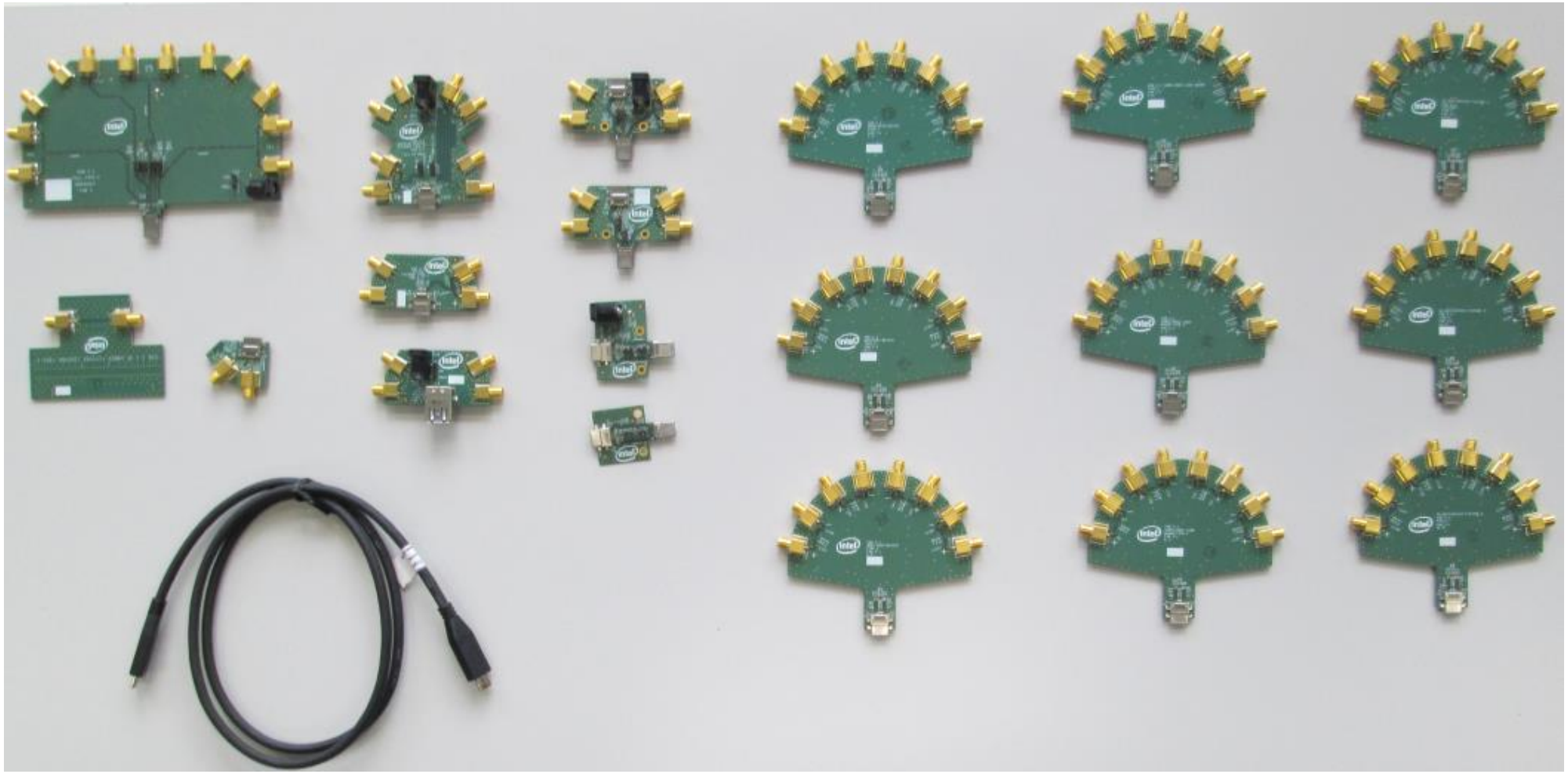
- Entry to the **Polling.Compliance** substate is described in Chapter 7. This initiates the transmission of the pseudo-random data pattern generated by the scrambled D0.0 compliance sequence. SKPs are not sent during the transmission of any compliance pattern.
- The **compliance pattern** shall be transmitted continuously or until a ping LFPS (refer to Section 6.9) is detected at the receiver.
  - Upon detection of a ping LFPS, the compliance pattern shall advance to the next compliance pattern.
  - Upon detection of a reset, LFPS the compliance pattern shall be terminated.
- In the table, patterns **CP0 through CP8 are transmitted at Gen 1 rate**, while **CP9 through CP16 are transmitted at Gen 2 rate**.

Table 6-14. Compliance Pattern Sequences

Compliance Pattern	Value	Description
CP0	D0.0 scrambled	A pseudo-random data pattern that is exactly the same as logical idle (refer to Chapter 7) but does not include SKP sequences.
CP1	D10.2	Nyquist frequency
CP2	D24.3	Nyquist/2
CP3	K28.5	COM pattern
CP4	LFPS	The low frequency periodic signaling pattern
CP5	K28.7	With de-emphasis
CP6	K28.7	Without de-emphasis
CP7	50-250 1's and 0's	With de-emphasis. Repeating 50-250 1's and then 50-250 0's.
CP8	50-250 1's and 0's	Without de-emphasis. Repeating 50-250 1's and then 50-250 0's.
CP9		Pseudo-random data pattern (see section 6.4.4.1)
CP10	AAh	Nyquist pattern at 10 Gb/s. This is not 128b132b encoded.
CP11	CCh	Nyquist/2 at 10 Gb/s, This is not 128b132b encoded.
CP12	LFSR15	Uncoded LFSR15 for PHY level testing and fault isolation. This is not 128b132b encoded. The polynomial is x^15+x^14+1.
CP13	64 1's and 0's	With pre-shoot defined in section 6.7.5.2 (no de-emphasis). Repeating 64 1's and then 64 0's at 10 Gb/s. This is not 128b132b encoded.
CP14	64 1's and 0's	With de-emphasis defined in section 6.7.5.2 (no pre-shoot). Repeating 64 1's and then 64 0's at 10 Gb/s. This is not 128b132b encoded.
CP15	64 1's and 0's	With pre-shoot and de-emphasis defined in section 6.7.5.2. Repeating 64 1's and then 64 0's at 10 Gb/s. This is not 128b132b encoded.
CP16	64 1's and 0's	No de-emphasis or pre-shoot. Repeating 64 1's and then 64 0's at 10 Gb/s. This is not 128b132b encoded.

Note: Unless otherwise noted, scrambling is disabled for compliance patterns.

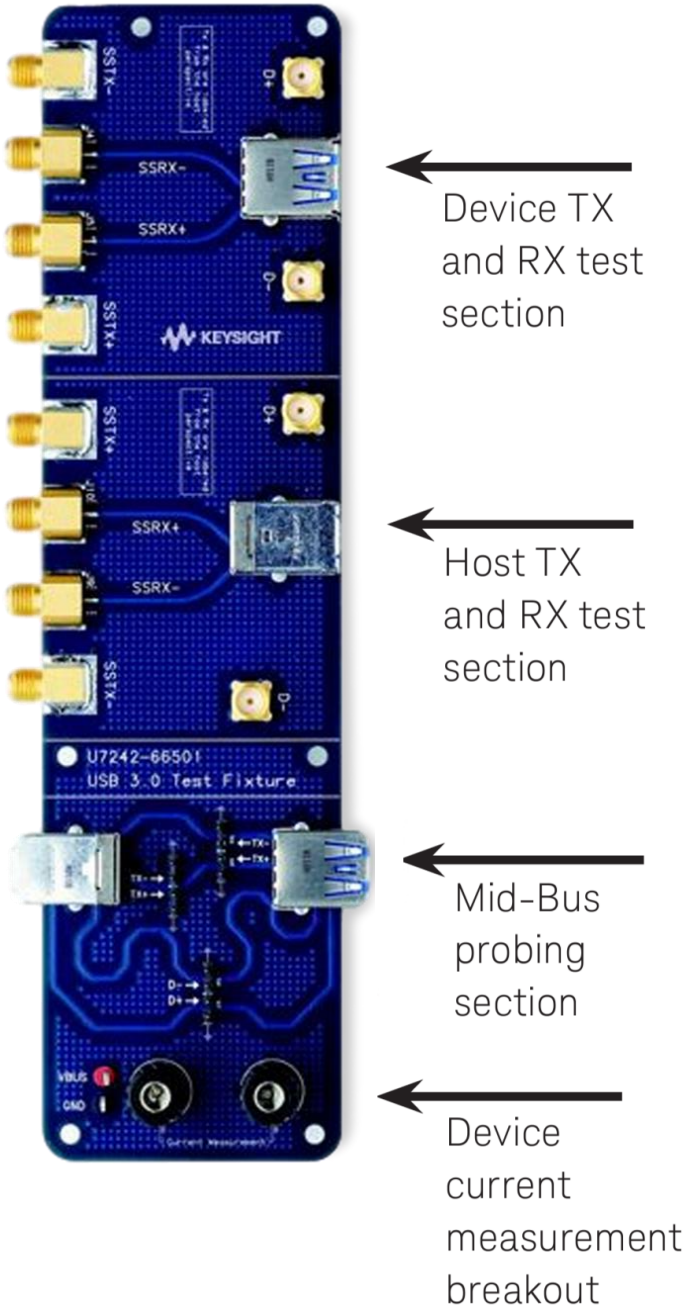
USB 3.2 Gen 2 Test Fixtures from USB-IF (up to 10 Gbit/s)



U7242A USB 3.0 Type-A/B Test Fixture

One test fixture for Host/Device/Mid-bus probing

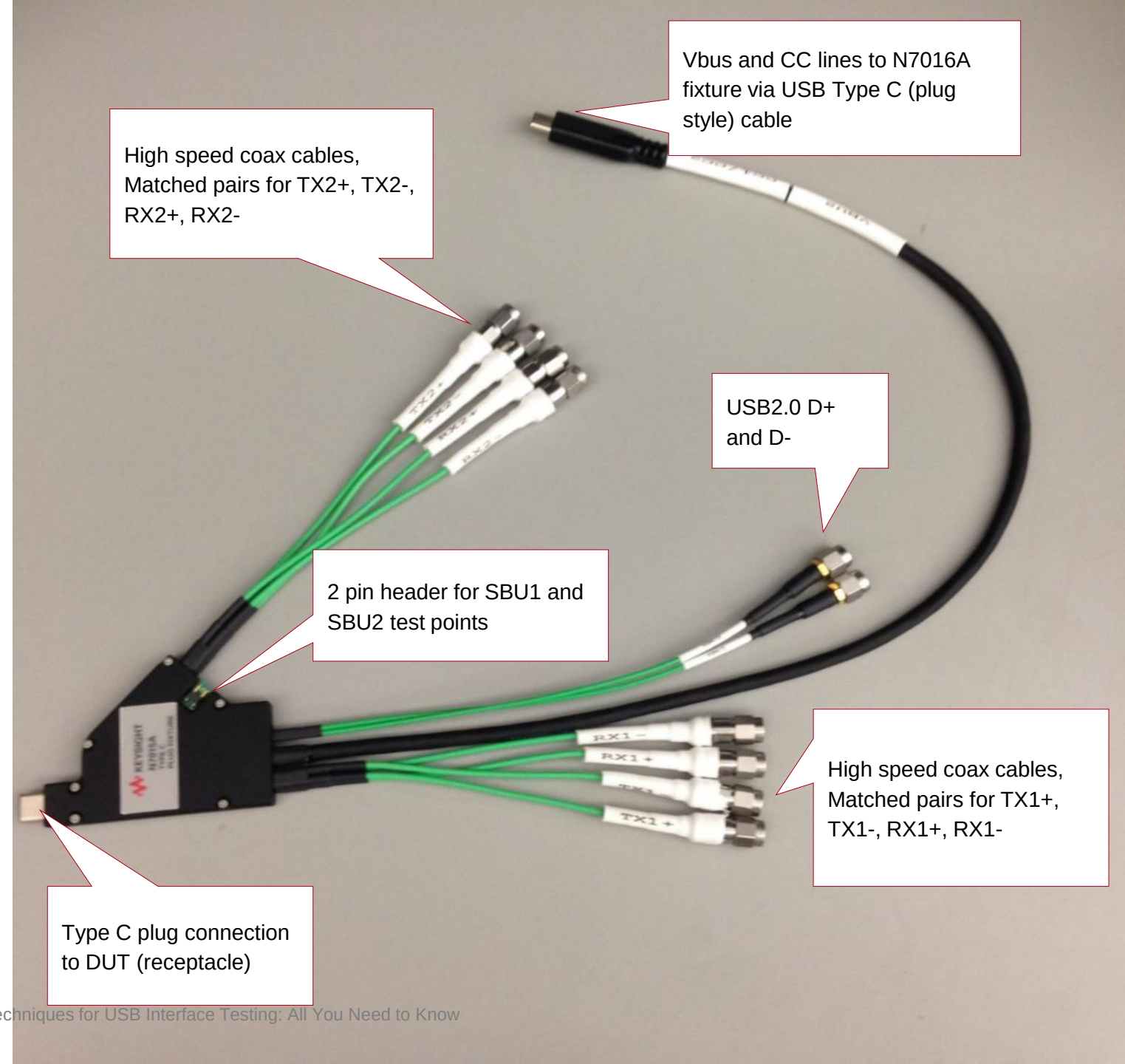
- Provides test point access for transmitter measurements
- Single-ended measurements as required by the USB 3.0 specification for transmitter and receiver validation and pre-compliance testing
- Differential measurements using active probes allow probing of active bus transactions for debug and verification testing
- USB 3.0 power probing features for easy measurement of transient and steady-state power states



N7015A Type-C Test Fixture

An easier way to test

- High speed (TX/RX) and D+/D- lanes accessible through coaxhigh-bandwidth cables
- S-parameters de-embedding models available and integrated into the USB/DP compliance applications and Infiniium baseline software
- SBU1/2 signals accessible for additional control purposes



N7018A Type-C Test Controller

N7018A: Power Delivery and Alt mode control as well as observability of CC, SBU lines, and V_{Bus}

Testing USB 3.2 Transmitters: Test Setup Example (USB-C)

Keysight Infiniium
Real-time oscilloscope

D9020USBC USB 3.2 Transmitter Compliance Test Application Software

D9020ASIA or **D9010DMBA** Advanced Signal Integrity Software

D9020JITA Jitter, Vertical and Phase Noise Analysis Software

DUT

3.5mm f/f adapters

TX1+/TX1-

RX1+/RX1- for toggling

Keysight
N7015A

USB-C cable

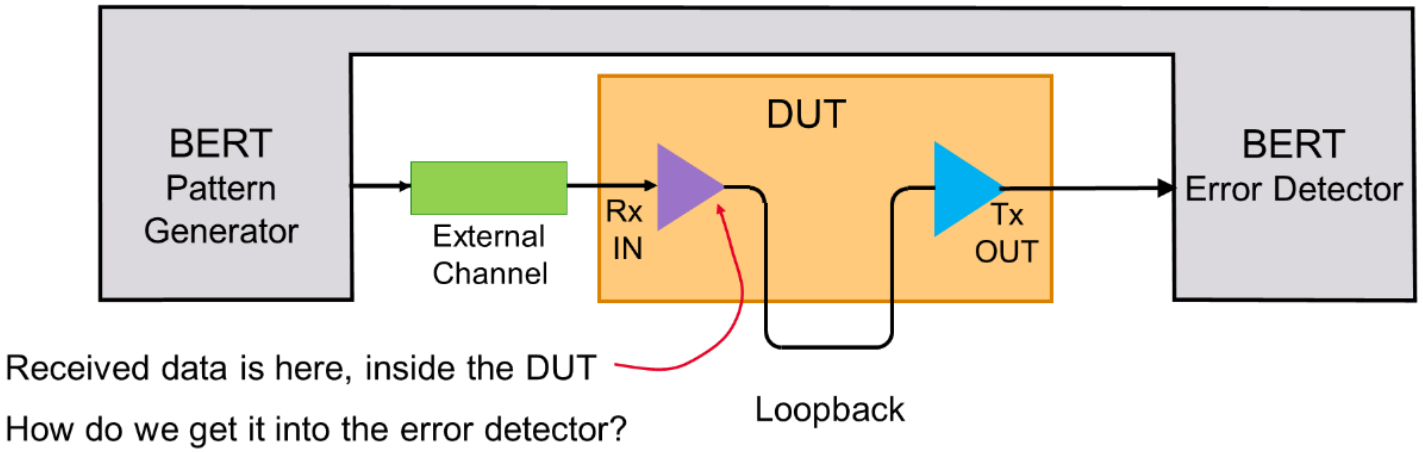
Keysight
N7018A USB-C controller

Power Supply (optional, if DUT is a power consumer)

Testing USB 3.2 Receivers: What is the Concept?

An RX test is performed to determine an RX's capability to properly detect the digital signal content, even for a worst-case impaired analog input signal

1. A Pattern Generator (PG) is used to emulate a system's TX plus channel thus **generating a data signal containing the impairments** to be expected at the RX input when operating in a target system. This signal must be **calibrated** to specified values residing in a specified setup.
2. The RX under test is set into an appropriate **test mode** and its input is stimulated with the calibrated signal residing in the specified **test set-up**
3. **Proper detection** of the digital content (i.e., the quality of the "A/D conversion") is monitored in a suitable fashion to determine the RX's performance **according to the target BER**



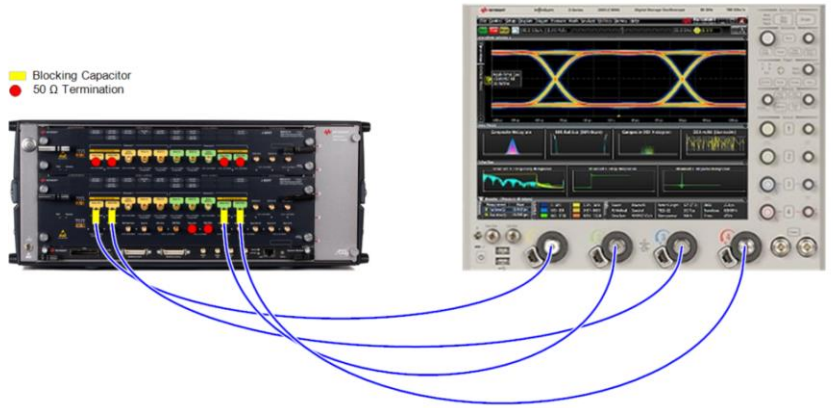
Testing USB 3.2 Receivers: Calibration Procedure Steps

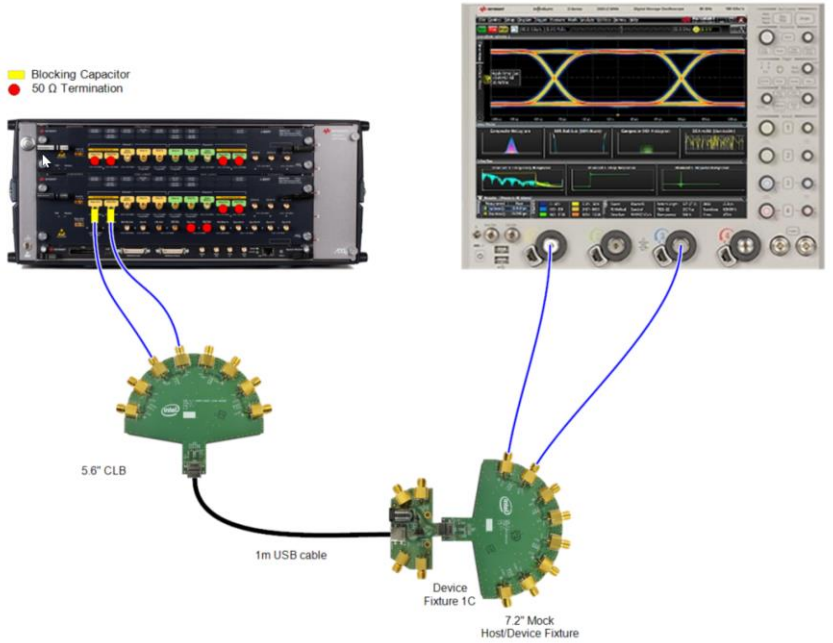
Without Test Channel

- Pre-shoot calibration
- De-emphasis calibration
- Generator output voltage calibration
- RJ calibration
- Low-frequency SJ calibration
- High-frequency SJ calibration

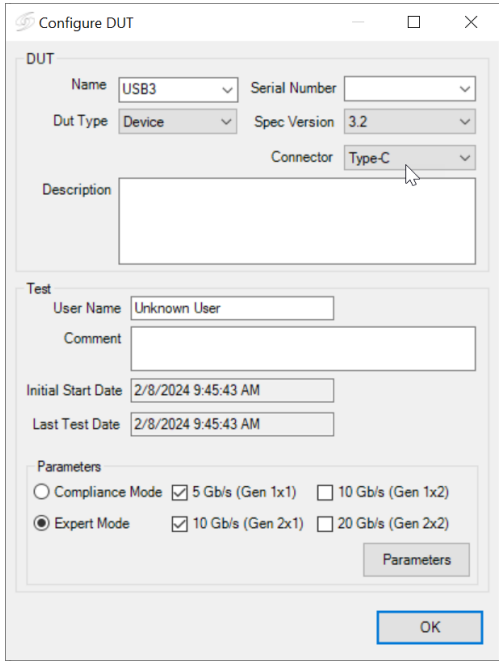
23 dB Channel (Long Channel):

- CLB selection
- Eye width pre-calibration
- Eye height and width calibration
- Compliance eye calibration
- Compliance eye verification



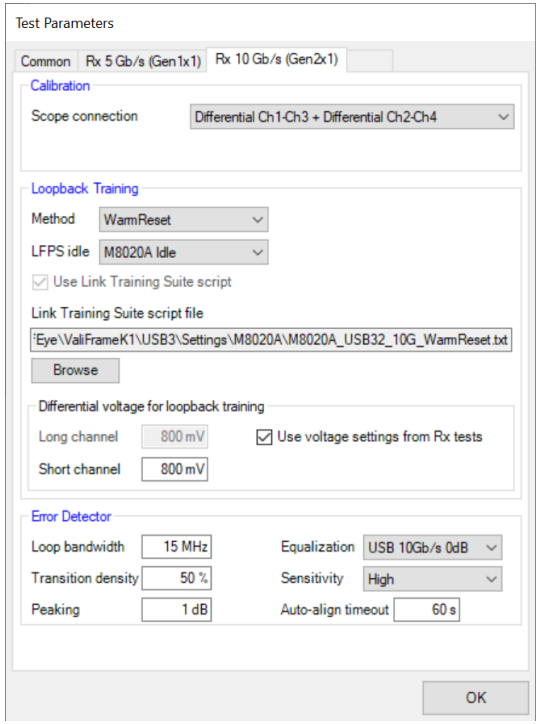


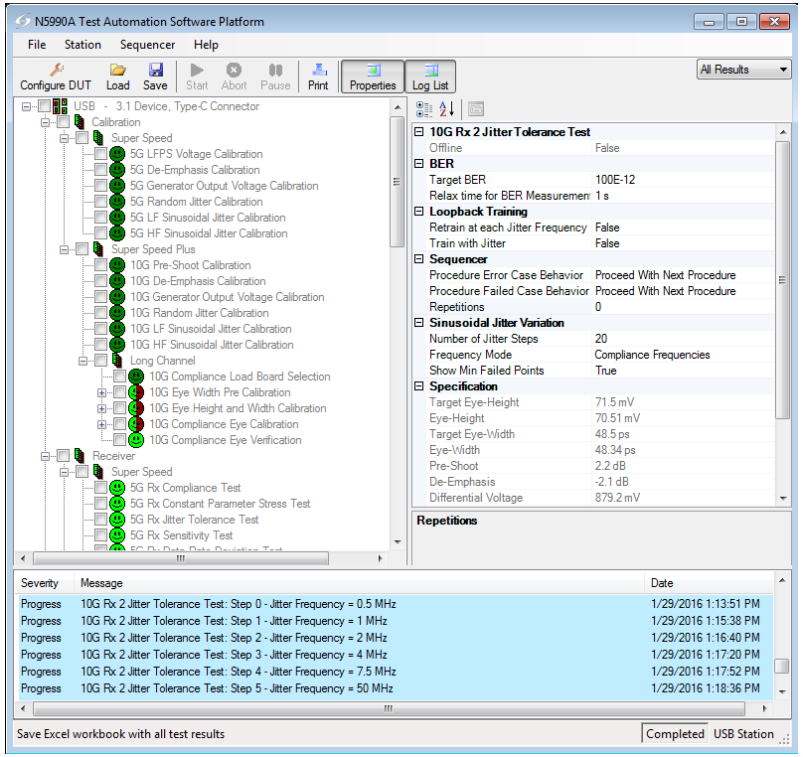
N5991U32A USB 3.2 Receiver Compliance Test Software



Setting up a DUT and test environment

BitifEye
Digital Test Solutions





[Link to the webpage of the N5991U32A USB 3.2 Receiver Compliance Test Software | Keysight]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